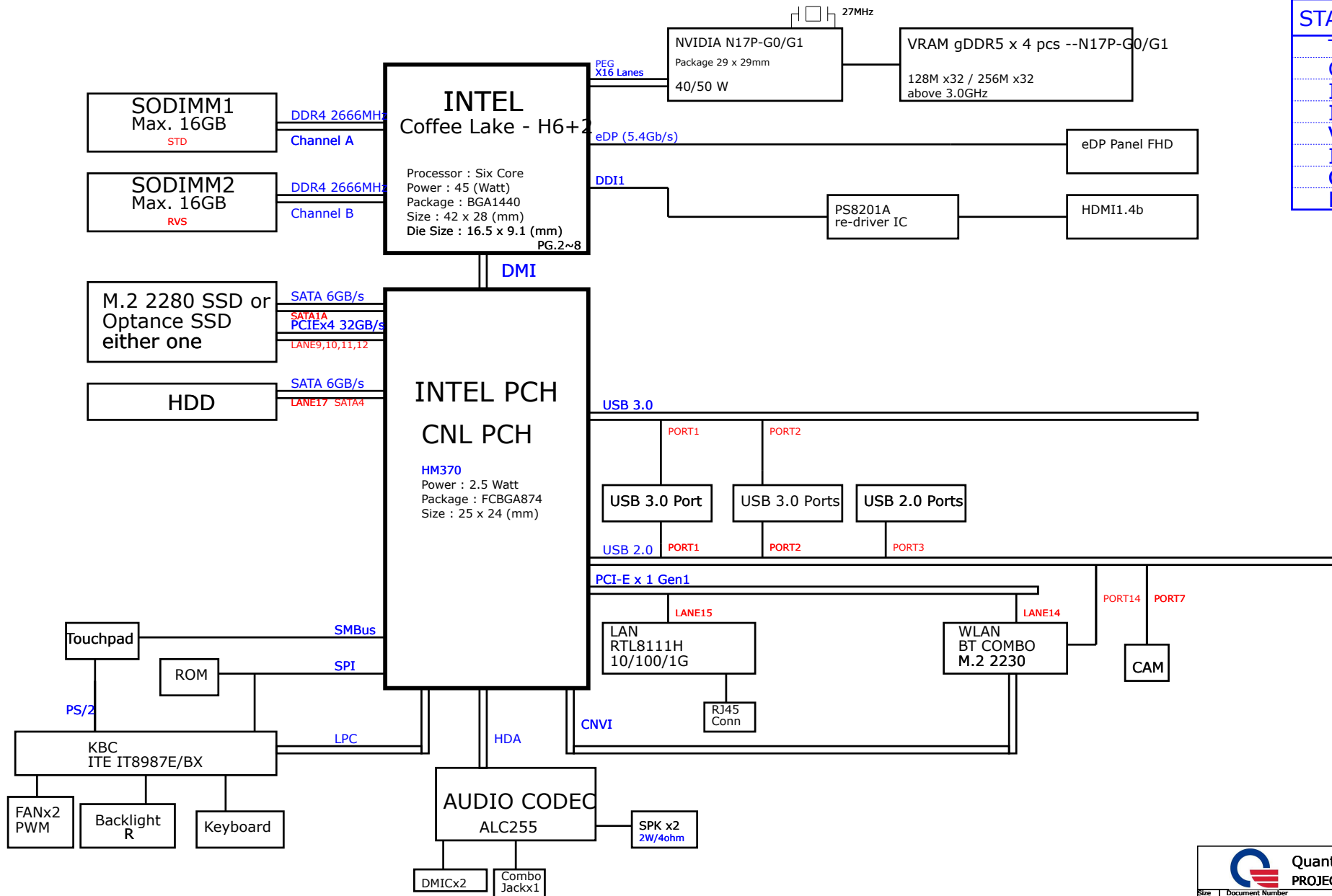


Asus 15" FX504 GD/GE Block Diagram

01

STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT



Model
FX504GD
FX504GE

REV

CHANGE LIST

ER

1124 Change

Page 10 OC3#/OC4#/OC5#/OC6#/OC7# to PU +3V_S5
Page 15 Reserved R1202 to isolate +1.05V_S5
Page 53 ADD I2R66/I2R68 for HDMI Pre-emphasis setting

1127 Change

Page 18 Reserved C221(DDR4_DRAMRST#)
Page 19 Reserved C260(DDR4_DRAMRST#)
Page 31 Modify HDD CONN CAP size to 0402 from 0201(C1234/C1235/C1232/C1233)
Page 31 Modify HDD CONN FP for "DFHS22FR522"
Page 32 Modify SSD CONN CAP size to 0402 from 0201(C318/C322/C323/C324/C325/C326/C327/C328)
Page 32 Modify WIFI CONN CAP size to 0402 from 0201(C338/C339)
Page 36 Modify "VPP_PG" to EC pin #126 from #19
Page 36 Modify "LED_CAP#" to EC pin #19 from #32
Page 36 Reserved EC pin #32 to TP(KTP51)
Page 36 Swap EC pin #77 & #76 signal "SPKER_ID" & "WLAN_RF_ON"
Page 23 Modify GPU timing(for GPU power sequence timing)
Page 50 ADD KB backlight PWM control
Page 13 Modify R1050 to 0ohm from 33ohm

1101 Change

Page 13 Modify SML3ALERT#/SML2ALERT# PU to +3V_S5 from +3V
Page 36 Modify SPI damping resistor to 33ohm from 15ohm
Page 36 Modify MB ID Pin Define("MB_ID1"/"MB_ID2")
Page 36 Modify SPK ID("SPK_ID0"/"SPK_ID1")

1204 Change

Page 7 Add +1.2V_S0 to VCCPLL_OC1/VCCPLL_OC2/VCCPLL_OC3
Page 34 Mount C350/C351 ,Modify R942/R941 to 2.2kohm from 4.7kohm (for adjust the touch pad I2C signal quality)
Page 34 ADD level shift for touch pad I2C

1205 Change

Page 16 ADD +1.2V_S0 & +1.05V_VCCSTG control form C10_POWER signal(Currently set is RUN_ON)
Page 20 ADD VC484(220pF) for DGPU_PWROK

1206 Change

Page 22 ADD RC(VR160/VR161 & VC480/VC481) for adjust the GPU I2C signal quality
Page 30 Reserved ESD(SD41 & SD42) component for USB_ON

1124 Change

Page 10 OC3#/OC4#/OC5#/OC6#/OC7# to PU +3V_S5
Page 15 Reserved R1202 to isolate +1.05V_S5
Page 53 ADD I2R66/I2R68 for HDMI Pre-emphasis setting

1127 Change

Page 18 Reserved C221(DDR4_DRAMRST#)
Page 19 Reserved C260(DDR4_DRAMRST#)
Page 31 Modify HDD CONN CAP size to 0402 from 0201(C1234/C1235/C1232/C1233)
Page 31 Modify HDD CONN FP for "DFHS22FR522"
Page 32 Modify SSD CONN CAP size to 0402 from 0201(C318/C322/C323/C324/C325/C326/C327/C328)
Page 32 Modify WIFI CONN CAP size to 0402 from 0201(C338/C339)
Page 36 Modify "VPP_PG" to EC pin #126 from #19
Page 36 Modify "LED_CAP#" to EC pin #19 from #32
Page 36 Reserved EC pin #32 to TP(KTP51)
Page 36 Swap EC pin #77 & #76 signal "SPKER_ID" & "WLAN_RF_ON"
Page 23 Modify GPU timing(for GPU power sequence timing)
Page 50 ADD KB backlight PWM control
Page 13 Modify R1050 to 0ohm from 33ohm

1101 Change

Page 13 Modify SML3ALERT#/SML2ALERT# PU to +3V_S5 from +3V
Page 36 Modify SPI damping resistor to 33ohm from 15ohm
Page 36 Modify MB ID Pin Define("MB_ID1"/"MB_ID2")
Page 36 Modify SPK ID("SPK_ID0"/"SPK_ID1")

1204 Change

Page 7 Add +1.2V_S0 to VCCPLL_OC1/VCCPLL_OC2/VCCPLL_OC3
Page 34 Mount C350/C351 ,Modify R942/R941 to 2.2kohm from 4.7kohm (for adjust the touch pad I2C signal quality)
Page 34 ADD level shift for touch pad I2C

1205 Change

Page 16 ADD +1.2V_S0 & +1.05V_VCCSTG control form C10_POWER signal(Currently set is RUN_ON)
Page 20 ADD VC484(220pF) for DGPU_PWROK

1206 Change

Page 22 ADD RC(VR160/VR161 & VC480/VC481) for adjust the GPU I2C signal quality
Page 30 Reserved ESD(SD41 & SD42) component for USB_ON

PR

Page 10 ADD TP220 & TP221
Page 11 ADD RTC detect (R12475/R1216/Q50/R1217/R1218) for EC check .
Page 10 ADD R12474/ R12473 for SML1CLK & SML1DATA PU to +3V_S5.
Page 13 Modify (R1050/R1201/R1053) to short pad from 0ohm.
Page 14 Modify PR Board ID
Page 14 Reserve R1085 for DGPU_EVENT# PU
Page 14 Reserve R1088 for SMBALERT#(Strapping) set to "0"
Page 17 Reserve EMI CAP (EMC8/EMC9/EMC10/EMC11)
Page 23 Modify VC479 size to 0402 from 0201
Page 23 Modify VR67 to 150Kohm from 100kohm
Page 23 ADD VQ14/VR173/VC485(NVVDD_CORE1_EN)VQ15/VR174/VC486(1V8_MAIN_EN) for vGA power sequence.
Page 32 Modify C320 size to 0402 from 0201
Page 34 Modify TR2 to 18.7kohm from 10kohm for set TU1 temperature 125deg.
Page 34 Reserve TP die side PU R231 for TP_INTH#
Page 35 Modify (AR62/AR63/AR71) to short pad from 0ohm.
Page 36 Modify KR164 to 18.7kohm from 10kohm for set TU1 temperature 125deg.
Page 36 Reserve KC94 for PCH_SPI1_CLK_C
Page 40 Modify PR453 to 18.7kohm from 100kohm for set TU2 temperature 110deg.
Page 55 Modify ESD(LD7/LD8/LD10/LD9/LD1/LD2/LD5/LD6) P/N

DOC NO.

PROJECT MODEL :

BKLG/BKLN

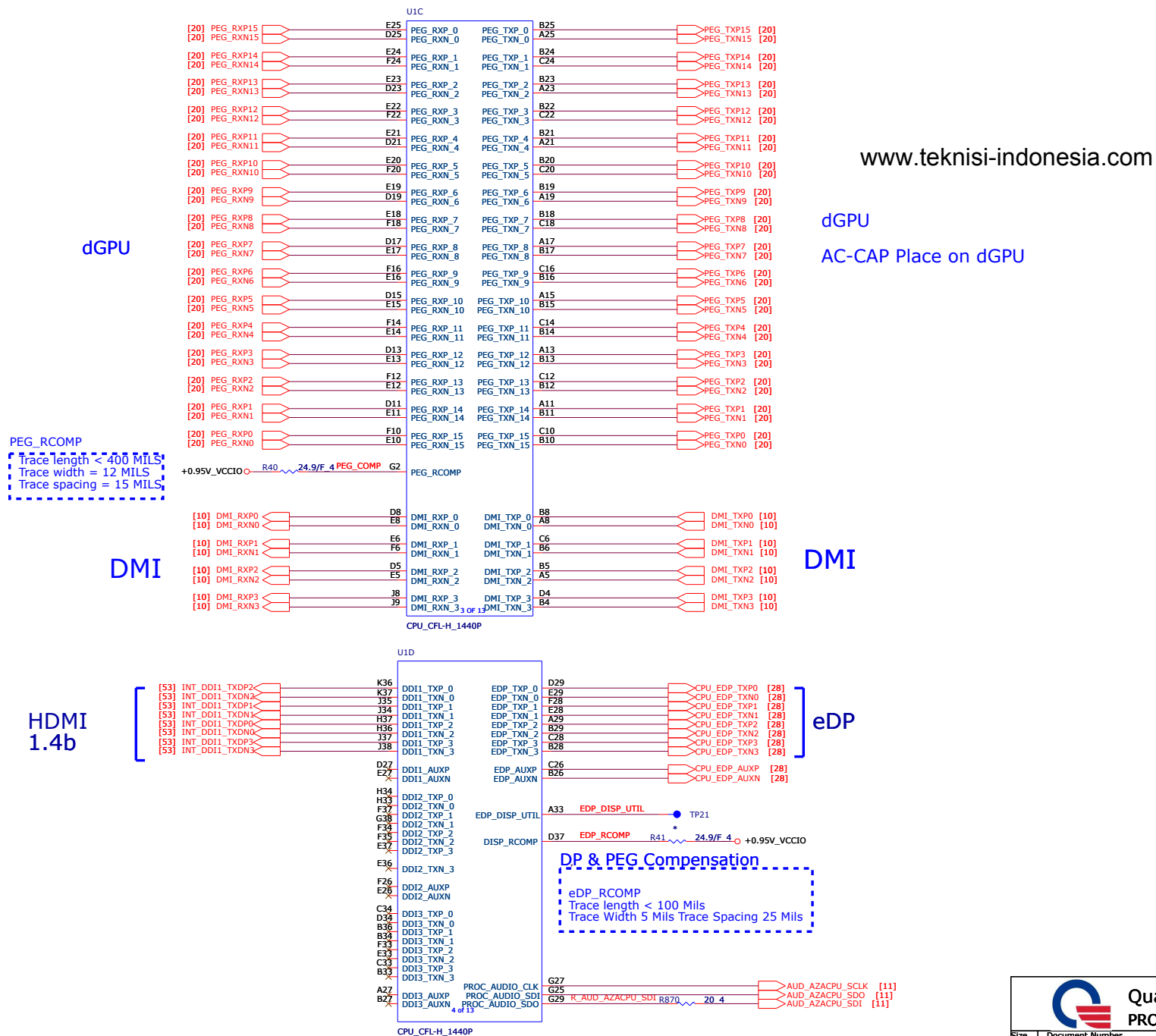
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DATE: 2018/01/17

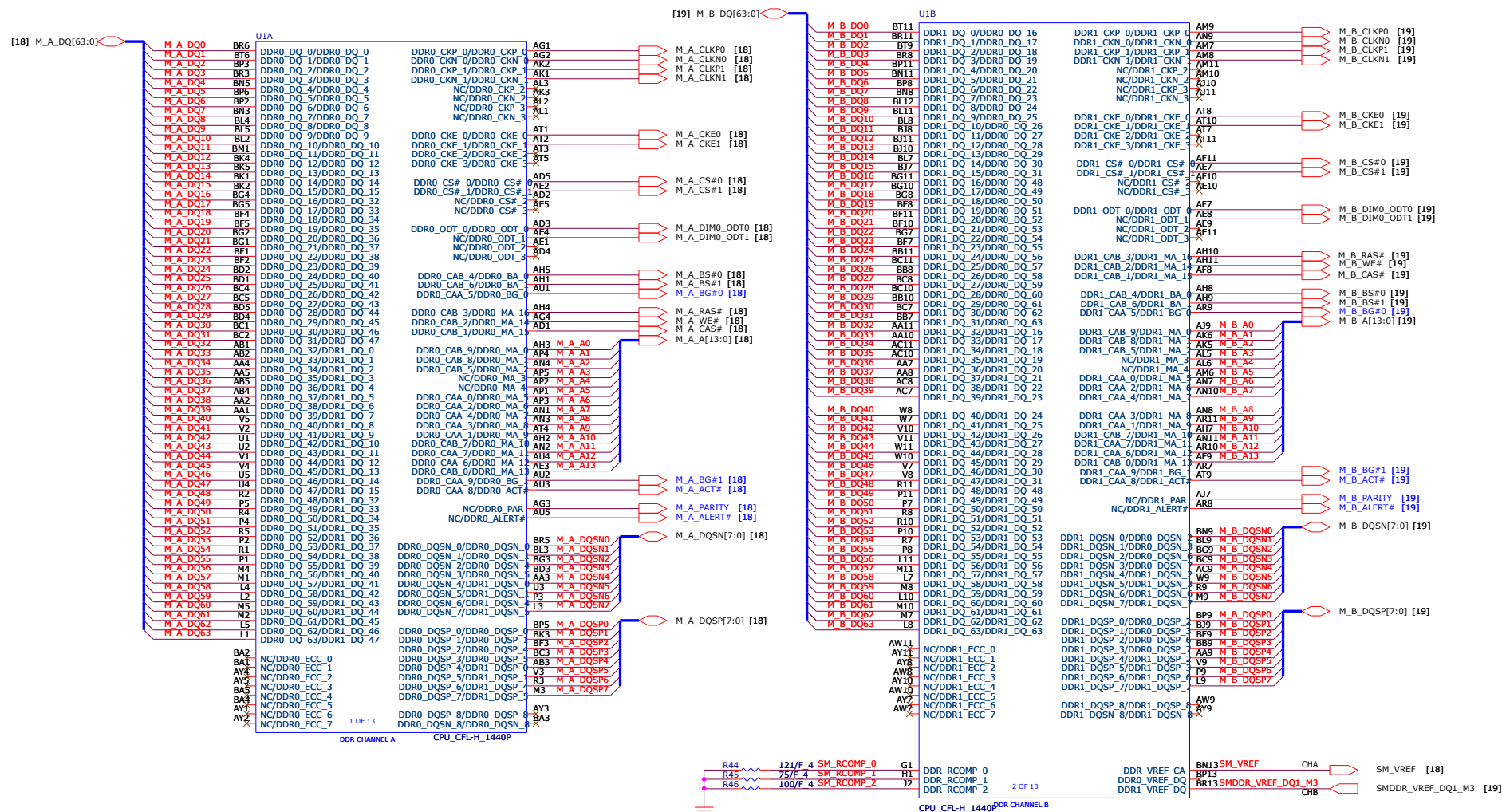
PART NUMBER:

DRAWING BY:

REVISION: 1A



Coffee Lake Processor (DDR4)

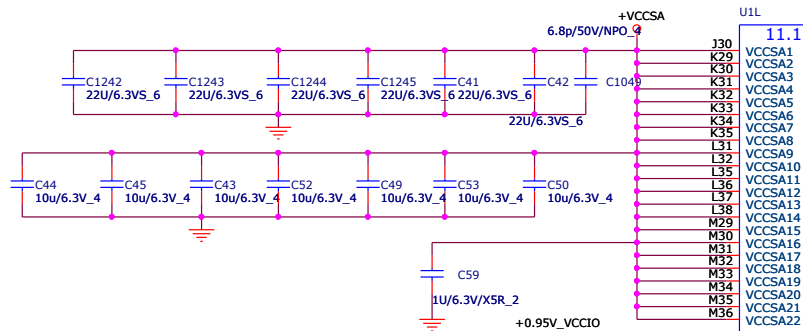


CFL Processor (POWER)

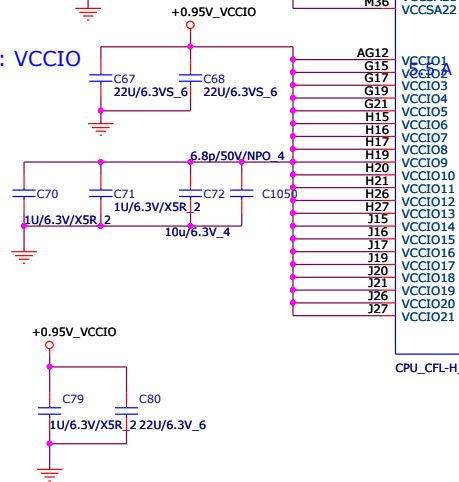
Follow CFL H page 126 to 45W(GT2): +VCCGT=34A



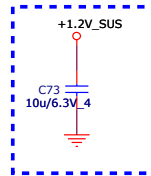
Follow CFL H EDS page 135 to 45W(GT2): VCCSA=11.1A



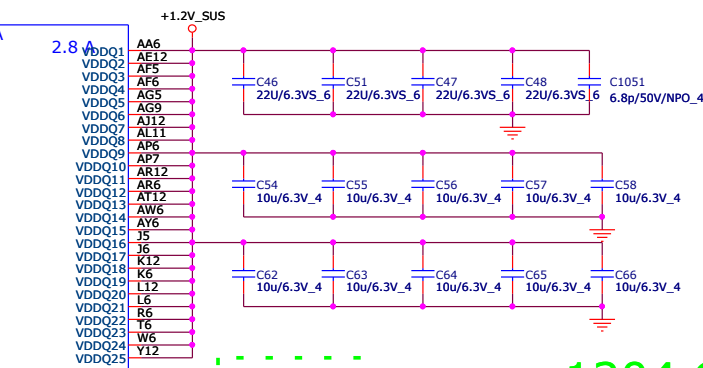
Follow CFL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V



Under CPU



Follow CFL H EDS page 135 45W: VDDQ=2.8A



0.26 A

0.12 A VCCST

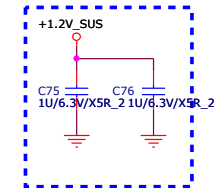
0.145 A

12 OF 13

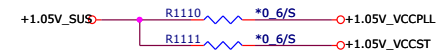
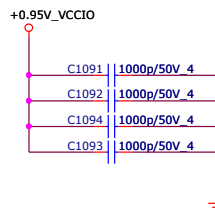
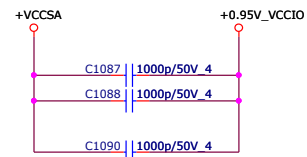
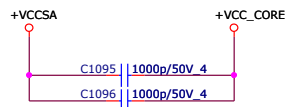
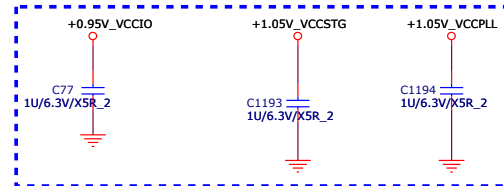
CPU_CFL-H_1440P

1204 Change

Close to U1.BH13/BJ13/G11

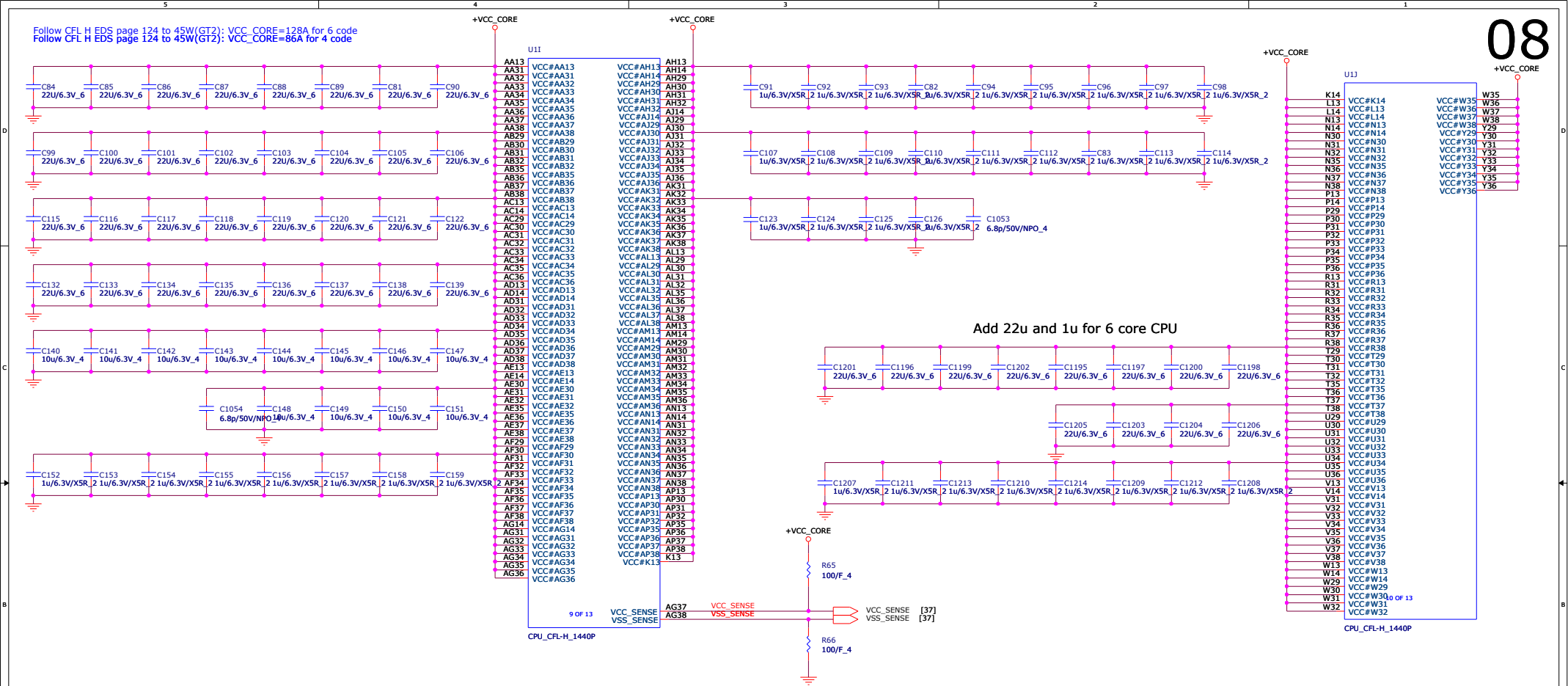


Close CPU



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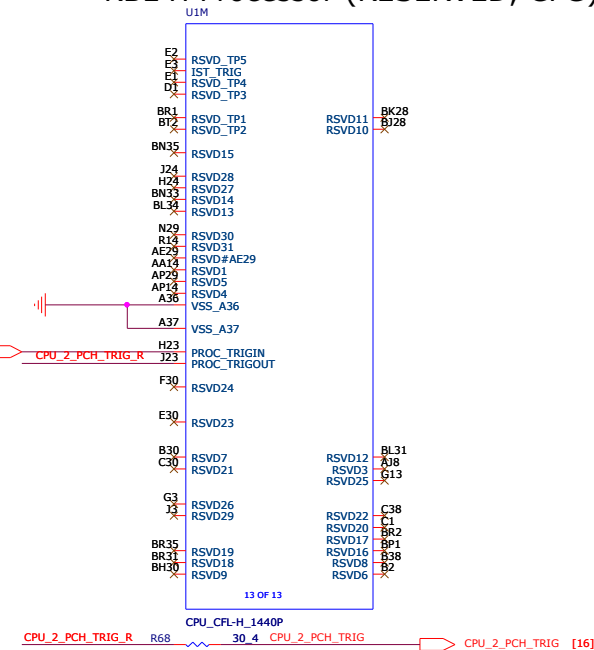
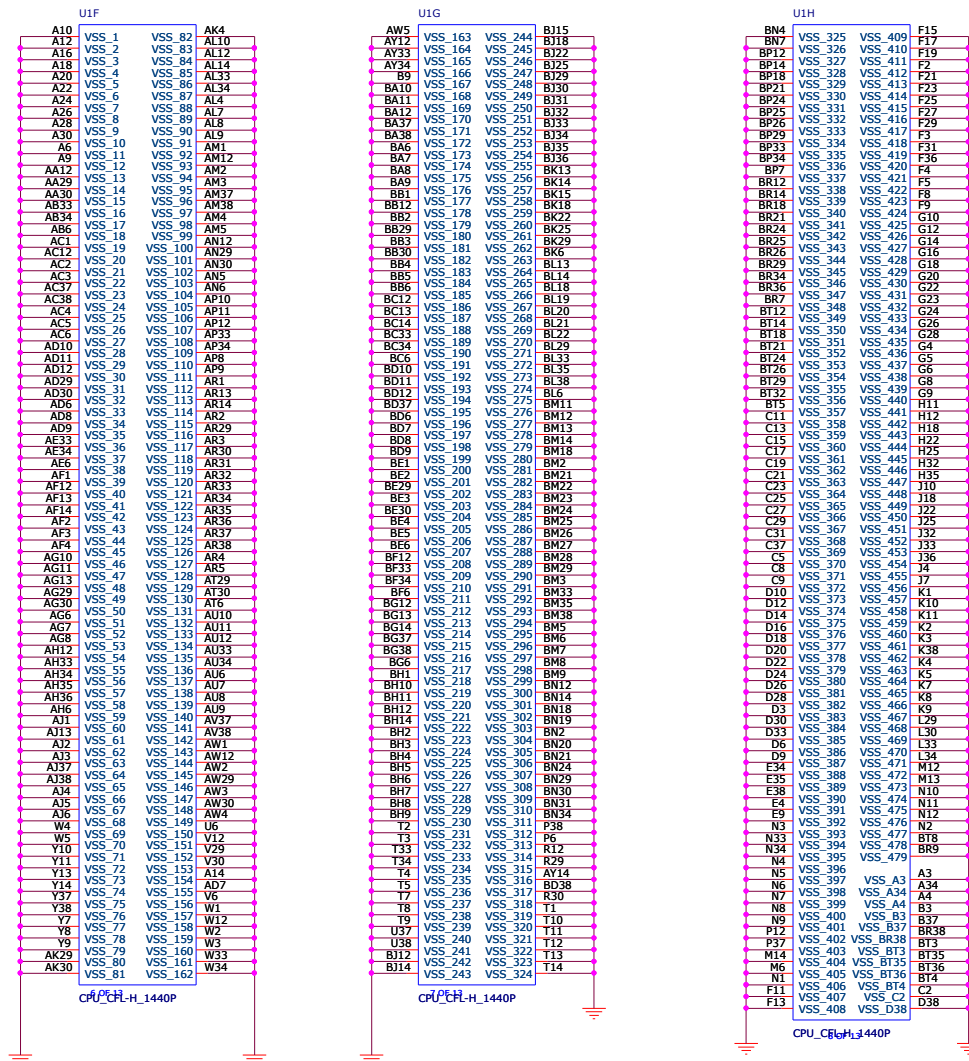
Follow CFL H EDS page 124 to 45W(GT2): VCC_CORE=128A for 6 code
Follow CFL H EDS page 124 to 45W(GT2): VCC_CORE=86A for 4 code

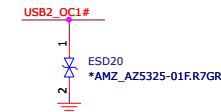


Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket
Trace Impedance 50 ohm

CFL-H Processor (GND)

KBL-H Processor (RESERVED, CFG)





If a USB port(s) is not implemented on the platform:
OC [x]# pins require a pull-up to V3.3A with 8.2k~10 K resistors



1/15 PR Change

DEVSPL: PCH O/D Output: DEV IPU



XDP_TDO_CPU R1109 51 4 +1.05V_VCCSTG

Close to PCH

DIFF FX504 GE

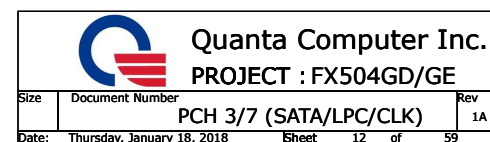
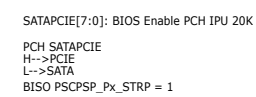


PR Chāngé

1208 ER Change

1/12 PR Change

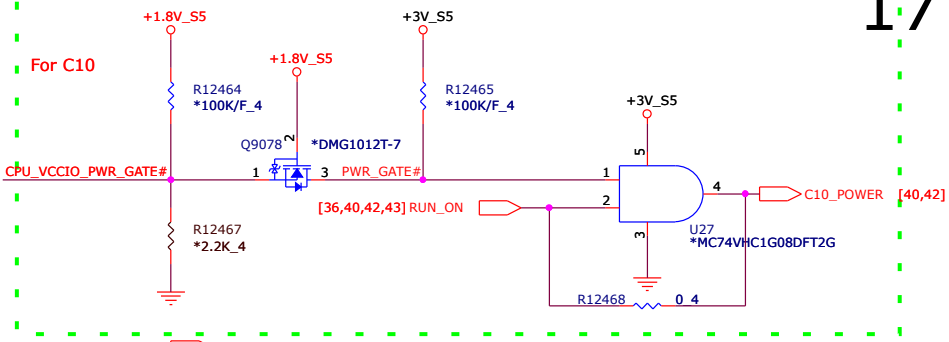
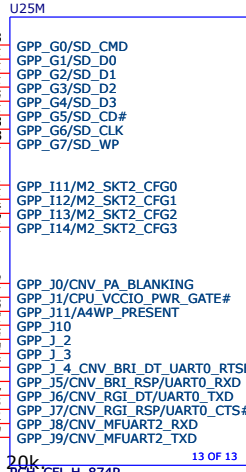
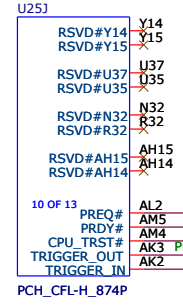
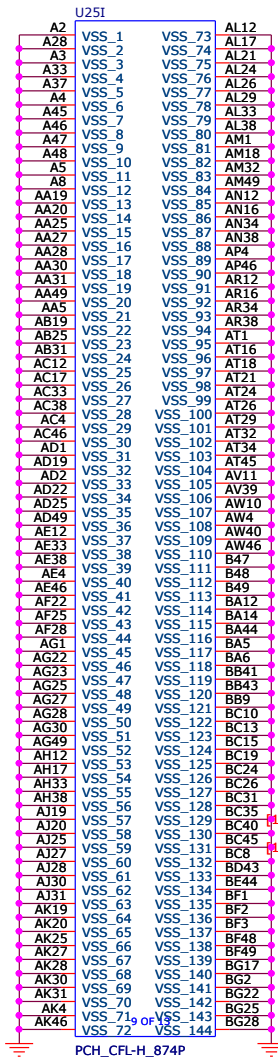
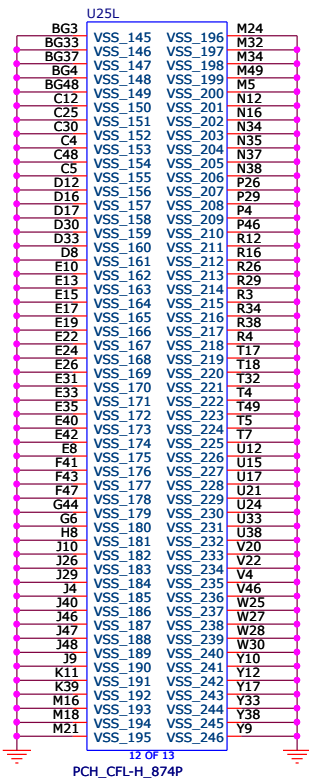
RTC Detect for EC Check



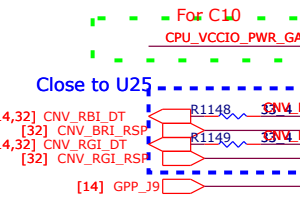
PR Change

DGPU_GC6_FB_EN R1084 10K 4
DGPU_EVENT# R1085 *10K 4

Note: If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

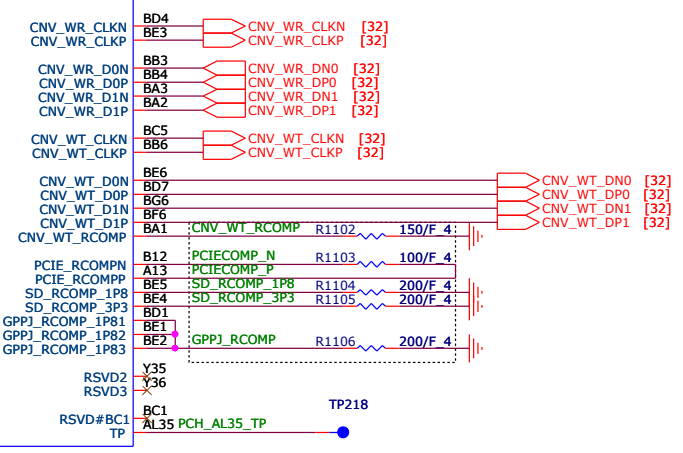


1205 Change

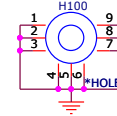
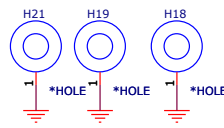
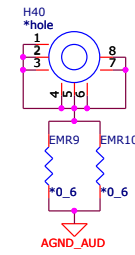
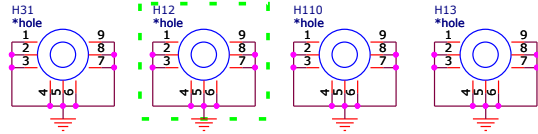


CNV_BRI_RSP : Model Internal Pull-UP 20K

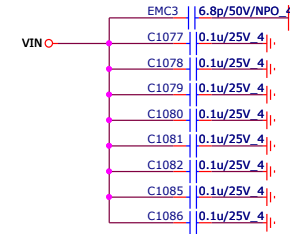
CNV_RGI_RSP : Model Internal Pull-UP 20K.



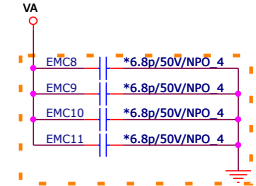
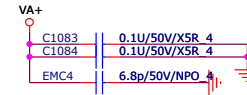
1207 Change



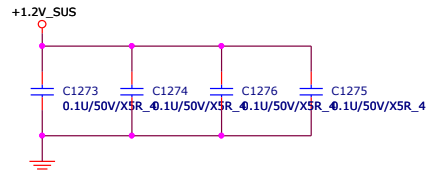
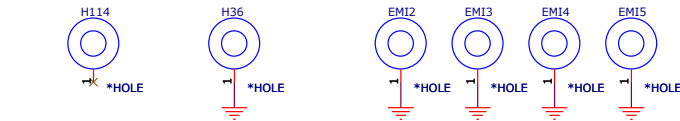
placement on TOP SIDE VIN Plane



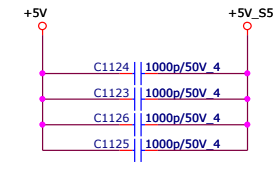
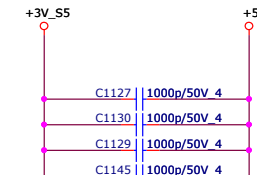
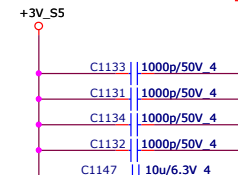
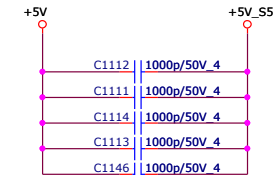
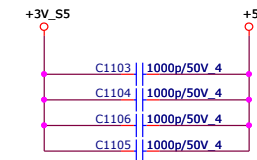
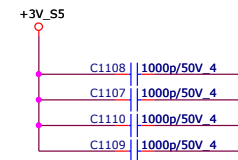
placement on TOP SIDE VA+ Plane



PR Change



For Over place use



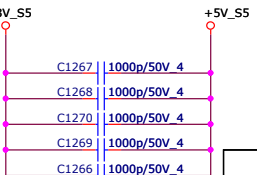
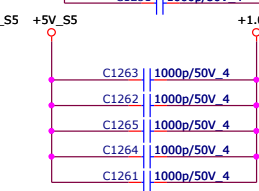
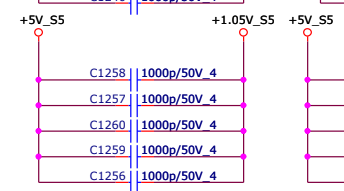
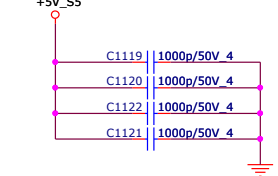
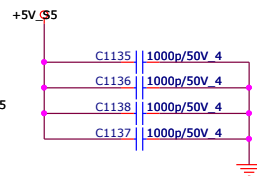
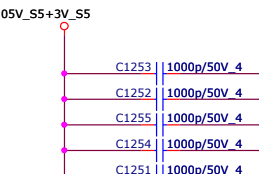
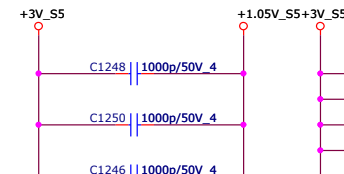
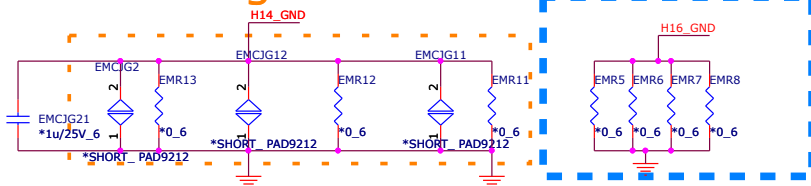
For EMC

For ESD request

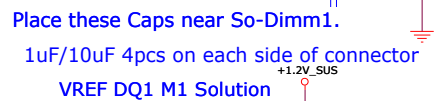
Close to H14

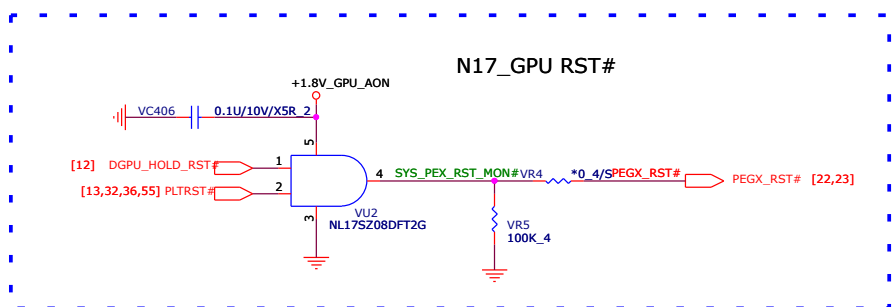
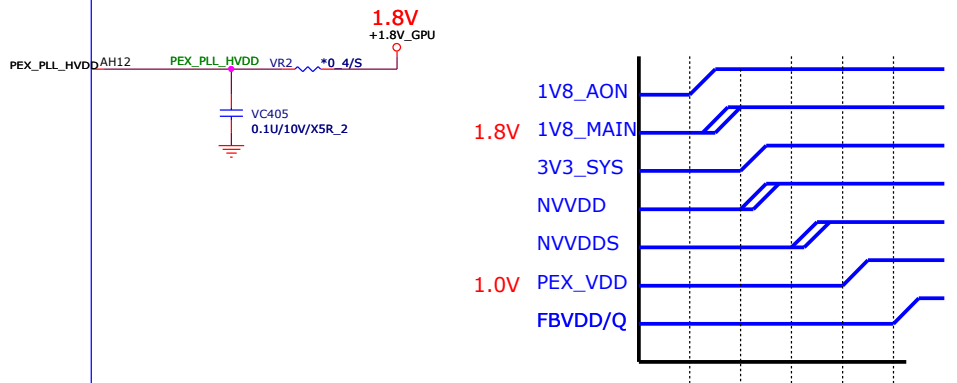
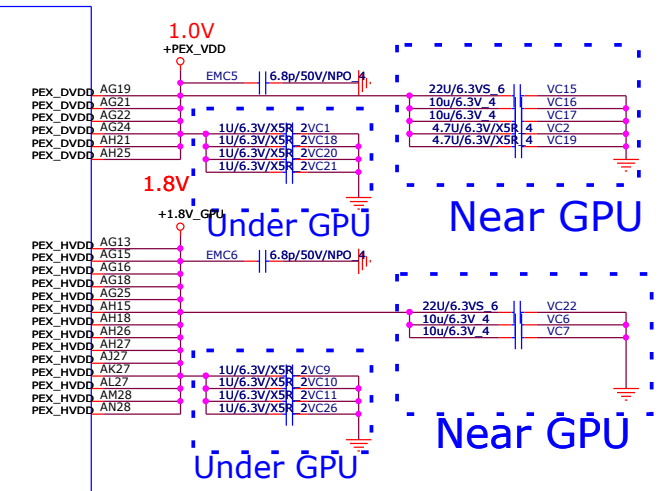
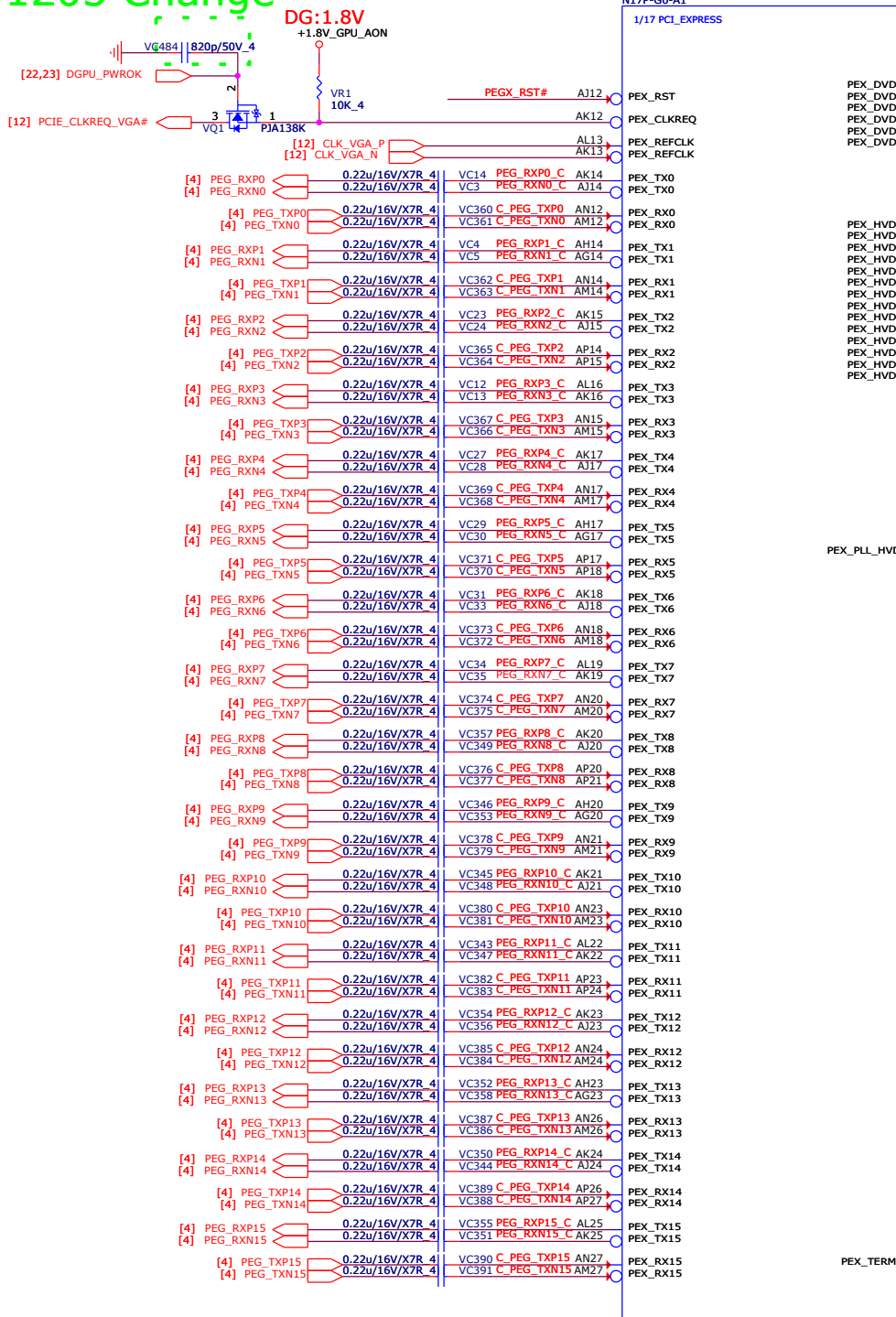
Close to H16

PR Change



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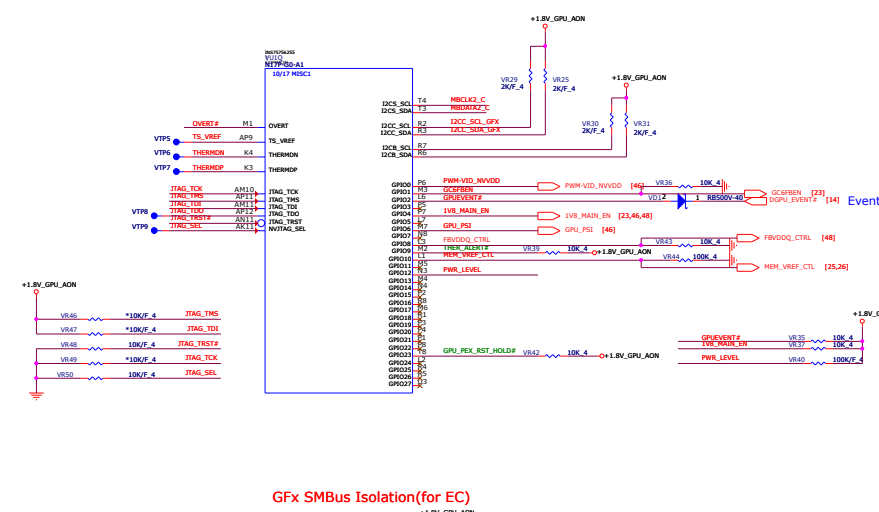
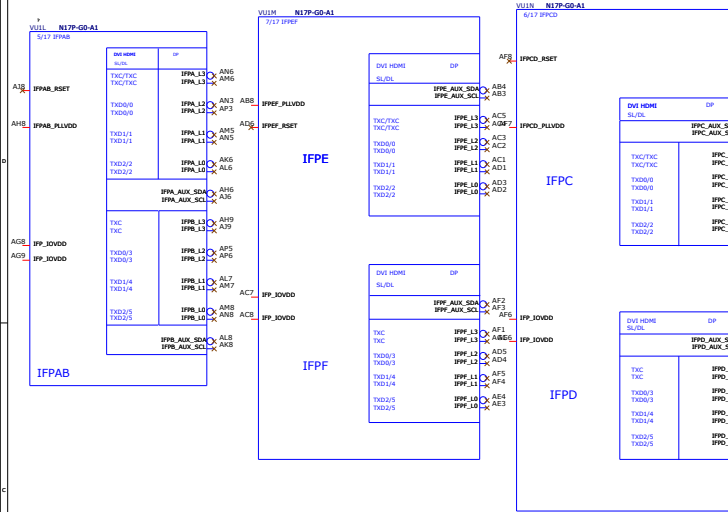


Table 14.2. GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVDDO_PWL_VID	O	PWM Output to control NVDDO	0 to V8 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 kΩ pull-down
GPIO2	GC6M: GPU_EVENT7/ WAKE	I	GPU wake signal for GC6 2.1	10KΩ pull-up to V8_AON, unless driven actively.
GPIO3	NVDDO_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to V8 output
GPIO4	GC6M: V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain V8 pull-up to V8AON

Table 14.2. GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVDDO_PSI	O	Phase Shidding (see Section 14.3.3)	10 kΩ pull-up to V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDDO_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDDO power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDDO	O	Quadro: Power_Brakof	Panel Power enable 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or Power supply overdraw input	100 kΩ pull-up to V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: GPU_PEX_RST_HOLDIF	O	System side PCIe reset monitor	10 kΩ pull-up to V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D_Vision	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	GC6S_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2. GPIO Descriptions for GB4C-128 Packages (Continued)

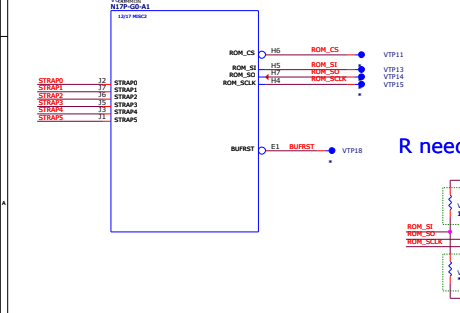
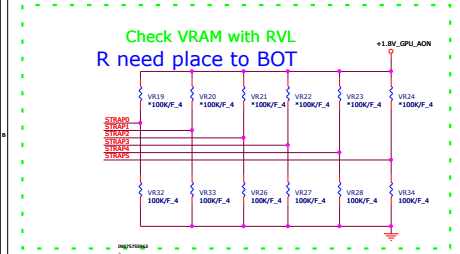
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6M: GPU_PEX_RST_HOLDIF	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to a gated V8
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5

STRAP[2:0] VRAM Table for N17P-G0/G1 GDDR5 Recommended Memories

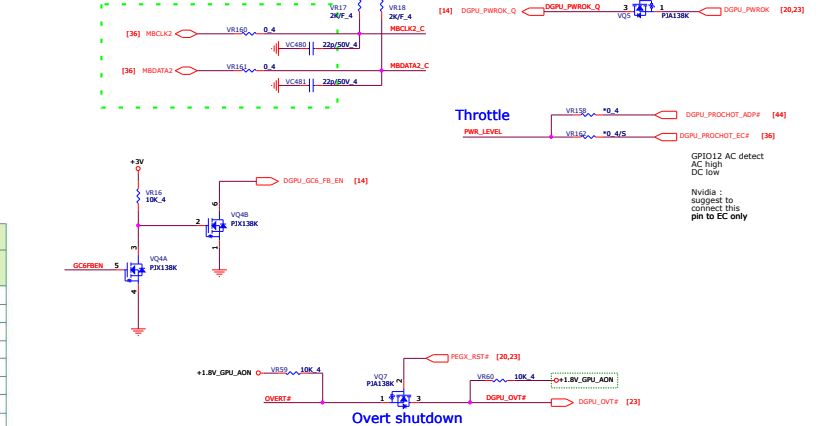
DESCRIPTION	Vendor	Quantia P/N	FBVDDQ
GDDR5 256Mx32 7 GHz	Samsung	K4G80325FB-HC28 (B-die)	1.5V/1.35V
GDDR5 256Mx32 7 GHz	Micro	MT51J256M32H-70:A (A-die)	1.5V/1.35V
GDDR5 256Mx32 7 GHz	Hynix	H5GC8H24MJR-R0C (M-die)	1.5V/1.35V
GDDR5 128Mx32 7 GHz	Samsung	K4G41325FE-HC28 (E-die)	1.5V/1.35V
GDDR5 128Mx32 7 GHz	Micro	EDW4032BABG-70-F-D (A-die)	1.5V/1.35V
GDDR5 128Mx32 7 GHz	Hynix	H5GC4H24AJR-R0C (A-die)	1.5V/1.35V

Table 5.3. RAMCFG

Strap Pins	Strap Pins	Strap Pins	RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)



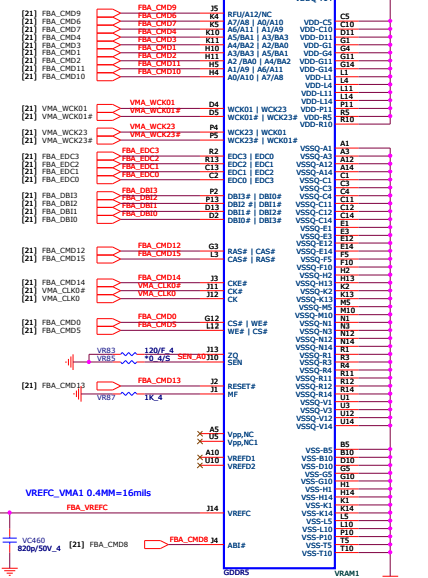
1206 Change



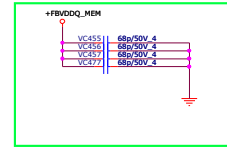
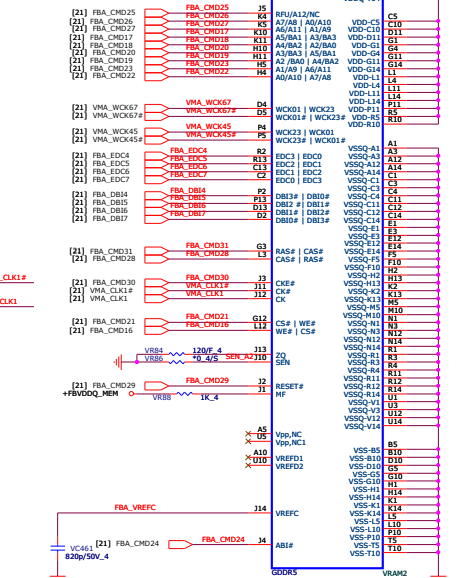
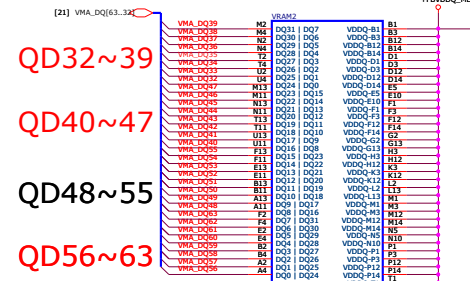
GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to V3V3_AON

Channel 0
<0-31>

MF=0 Non-mirrored

Channel 1
<32-63>

MF=1 mirrored



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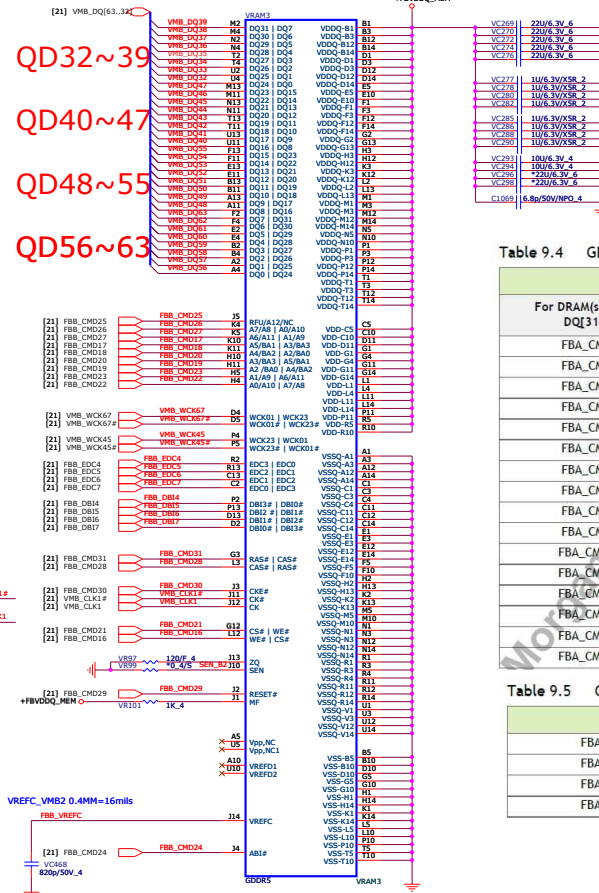
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	AB1*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

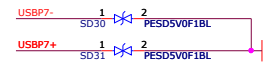
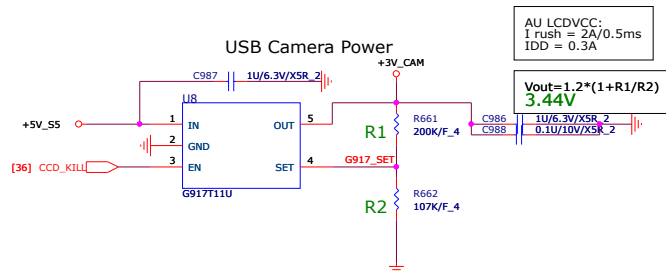
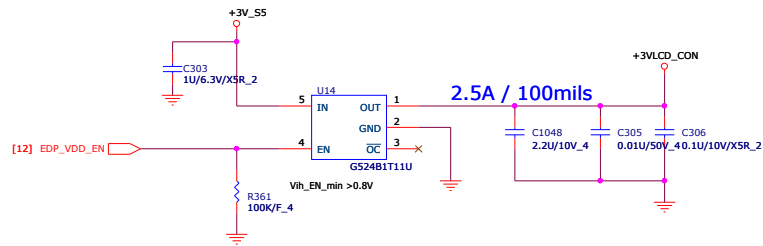
MF=1 mirrored



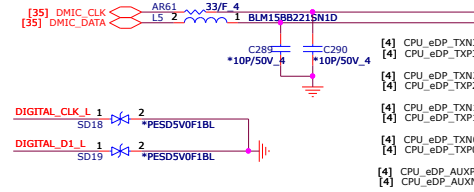
Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

D
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A

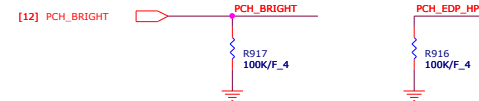
D
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A



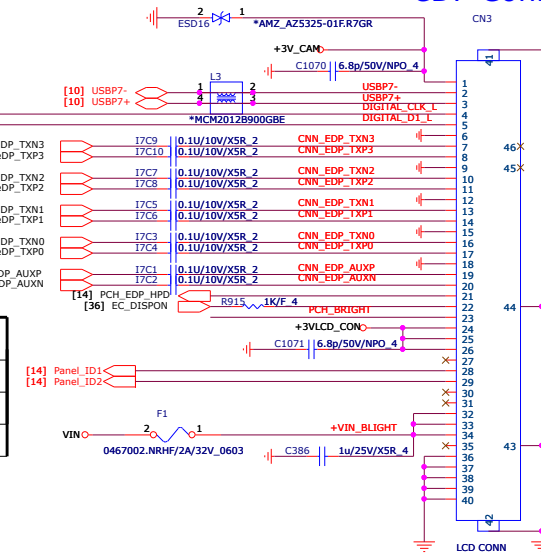
Camera



	Panel ID1	Panel ID2
FHD	1	1
4K2K	1	0
HD	0	1



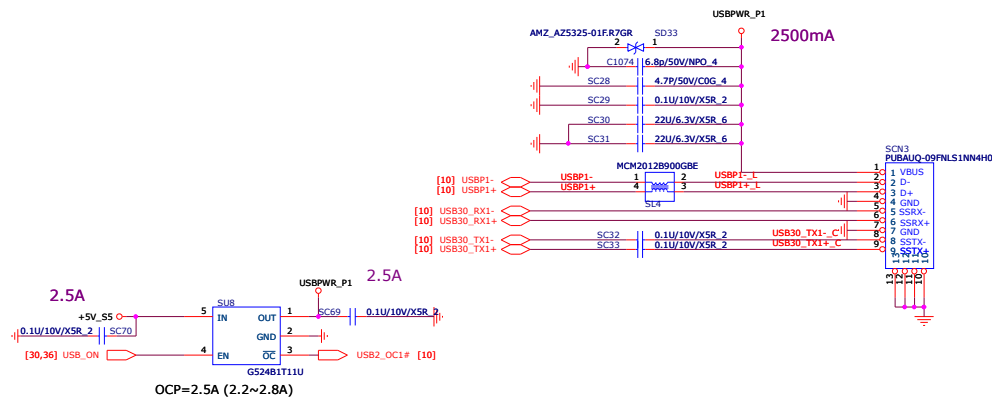
eDP Conn.



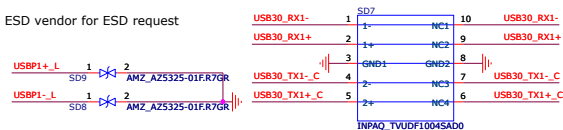
D
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D
C
B
A

USB 3.0 PORT1

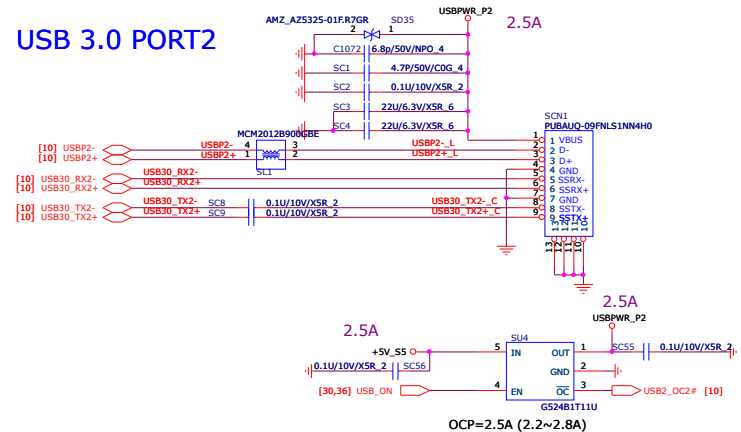


Change ESD vendor for ESD request

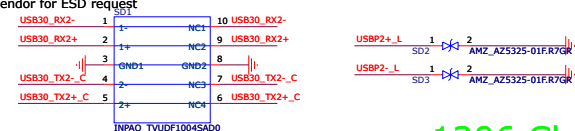


*Close to SCN3

USB 3.0 PORT2



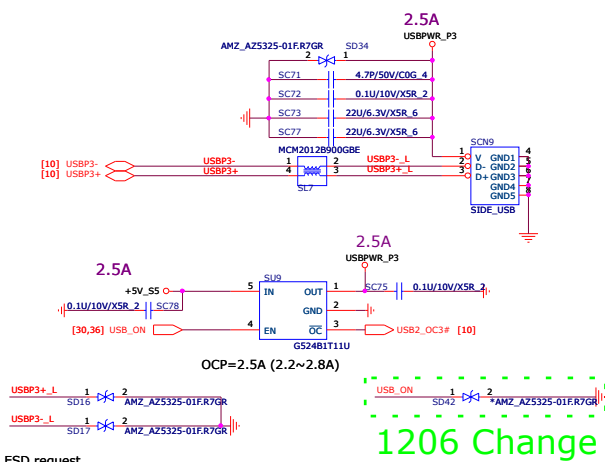
Change ESD vendor for ESD request



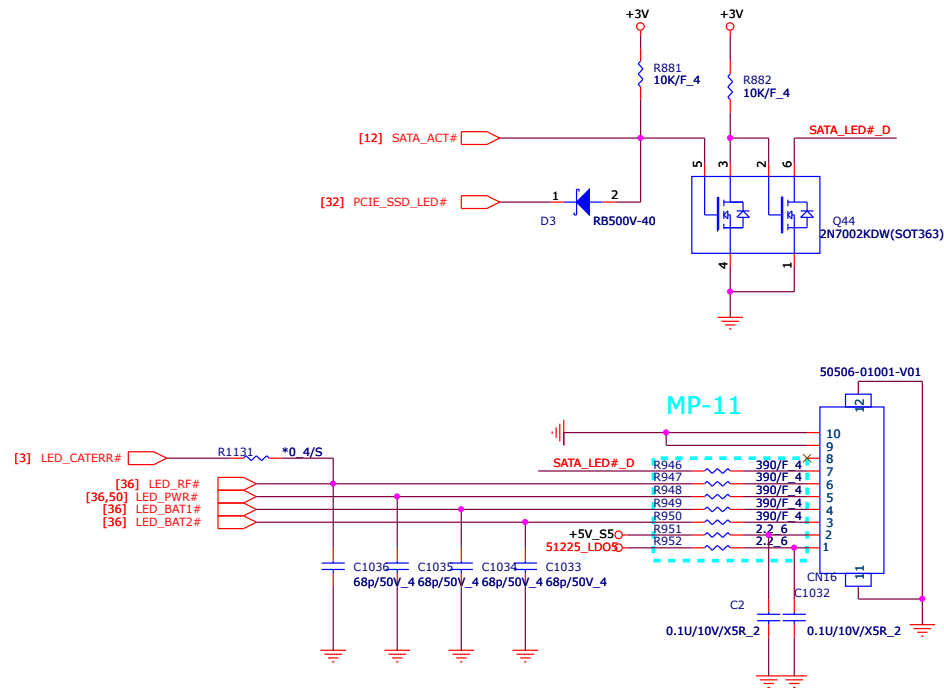
*Close to SCN1

1206 Change

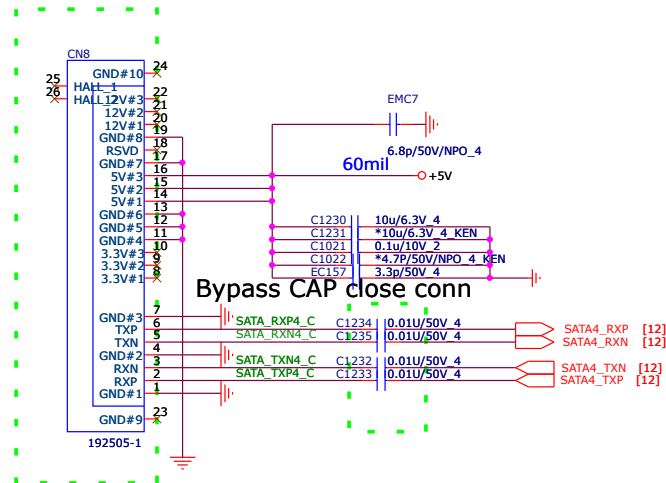
USB 2.0 PORT3



Change ESD vendor for ESD request



SATA HDD Connector



1127 Change



Quanta Computer Inc.
PROJECT : FX504GD/GE

SSD

1127 Change

Check again by Jay???

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WLAN/BT

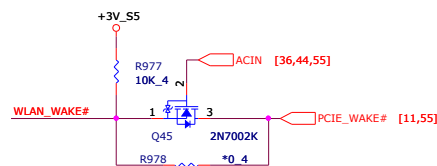
NGFF Wifi/BT (Hybrid Type E)

DRE(12-0004-01) RDC STD
DFHS75FR026

Blue Tooth

1127 Change

WIFI



AC Mode : Support wakle on LAN
DC Mode : Don't support wake on LAN

#571483 CRB Schematic
For Glitch Free Operation During Boot Process.
Signals Required Cap or Pull-Down Resistor
3.3V Signaling Mode = 100Kohm
1.8V Signaling Mode = 75Kohm

Follow #571483 CFL-H CRB0.9 Reserve Pull-H Resistor.

+1.8V_S5 R1137 *20K/F 4 CNV_BR1_RSP
+1.8V_S5 R1138 *20K/F 4 CNV_RGI_RSP

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466
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PAD

4 1:24:35

4

[36]

C340 *10p/50V/COG_4 CLK_24M_DEBUG

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PROJECT : FX304GD/

SSD/WLAN

Date: Thursday, January 18, 2018 Sheet 32 of 32

[illegible]

D

D

C

C

B

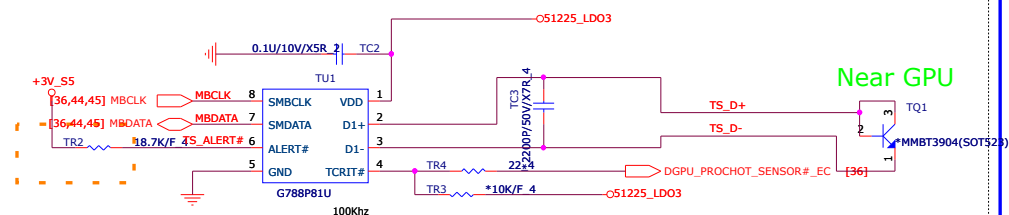
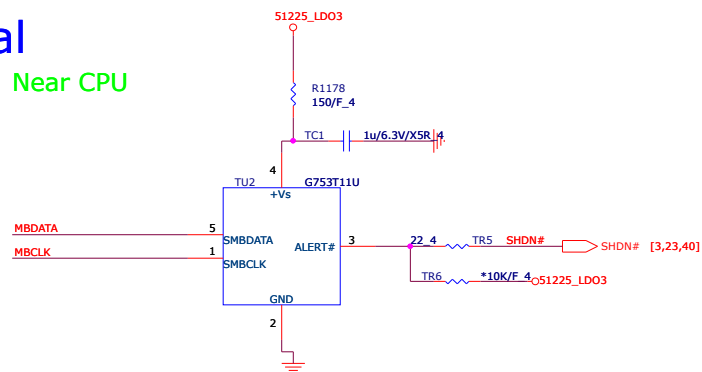
B

A

A

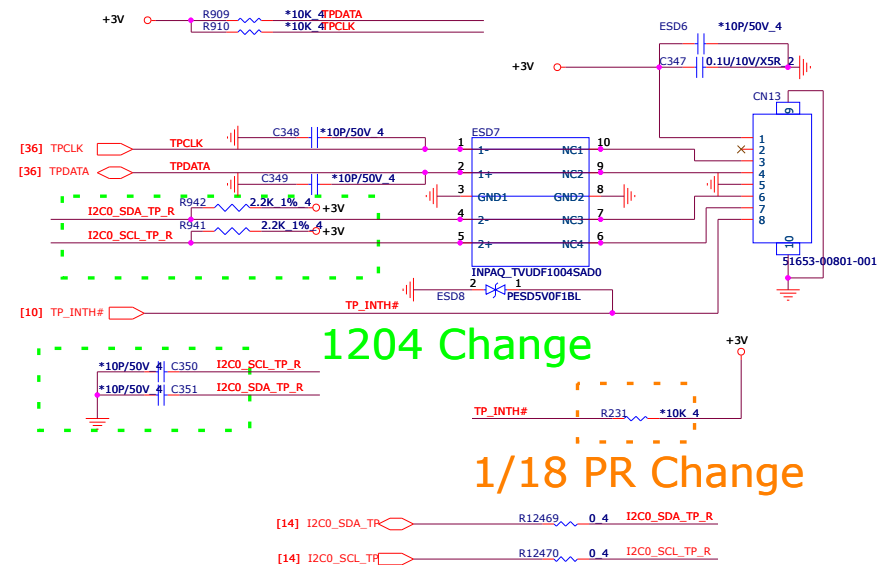
Thermal

Near CPU



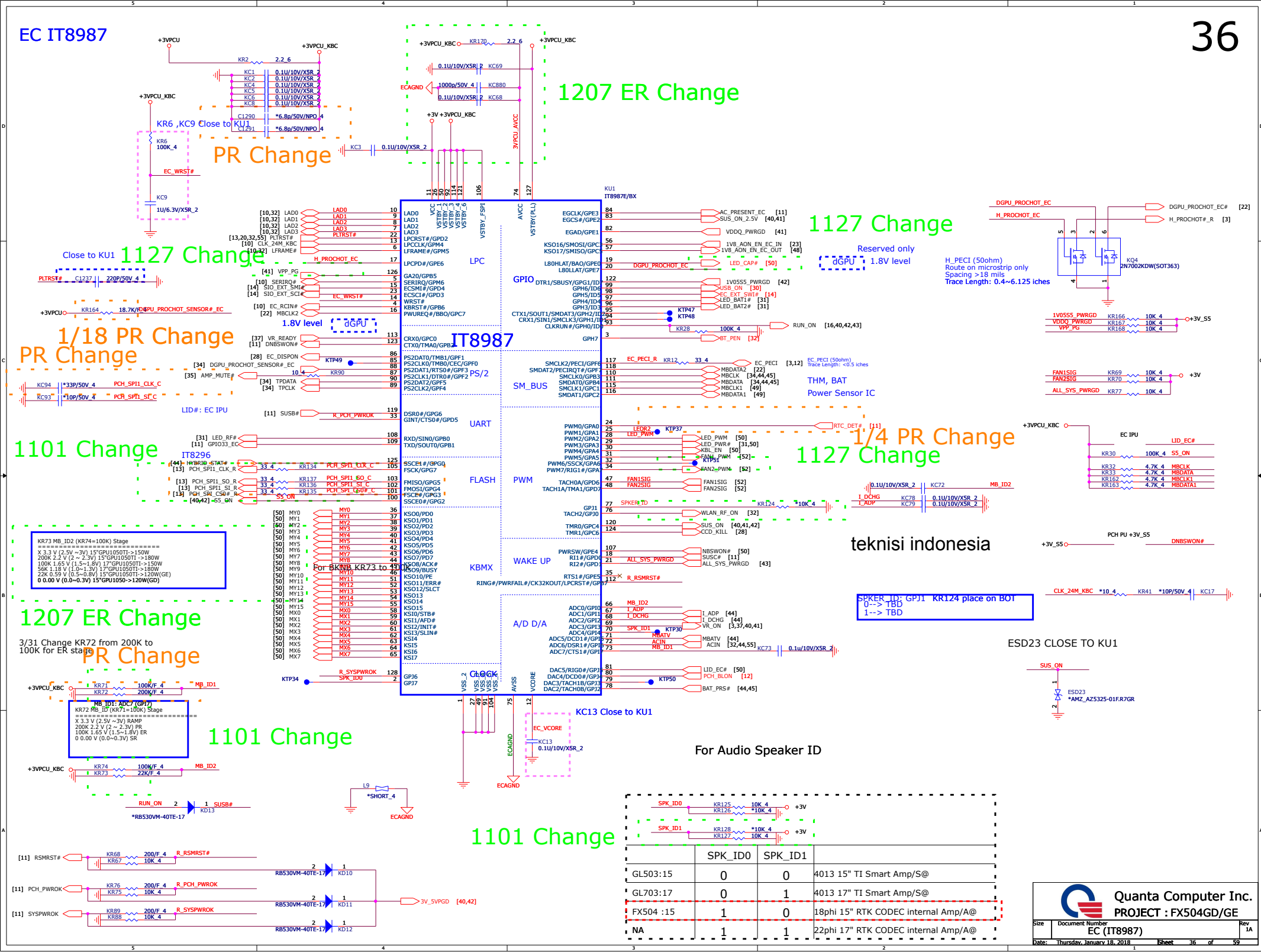
1/18 PR Change

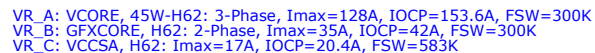
Touch Pad Connector AA type



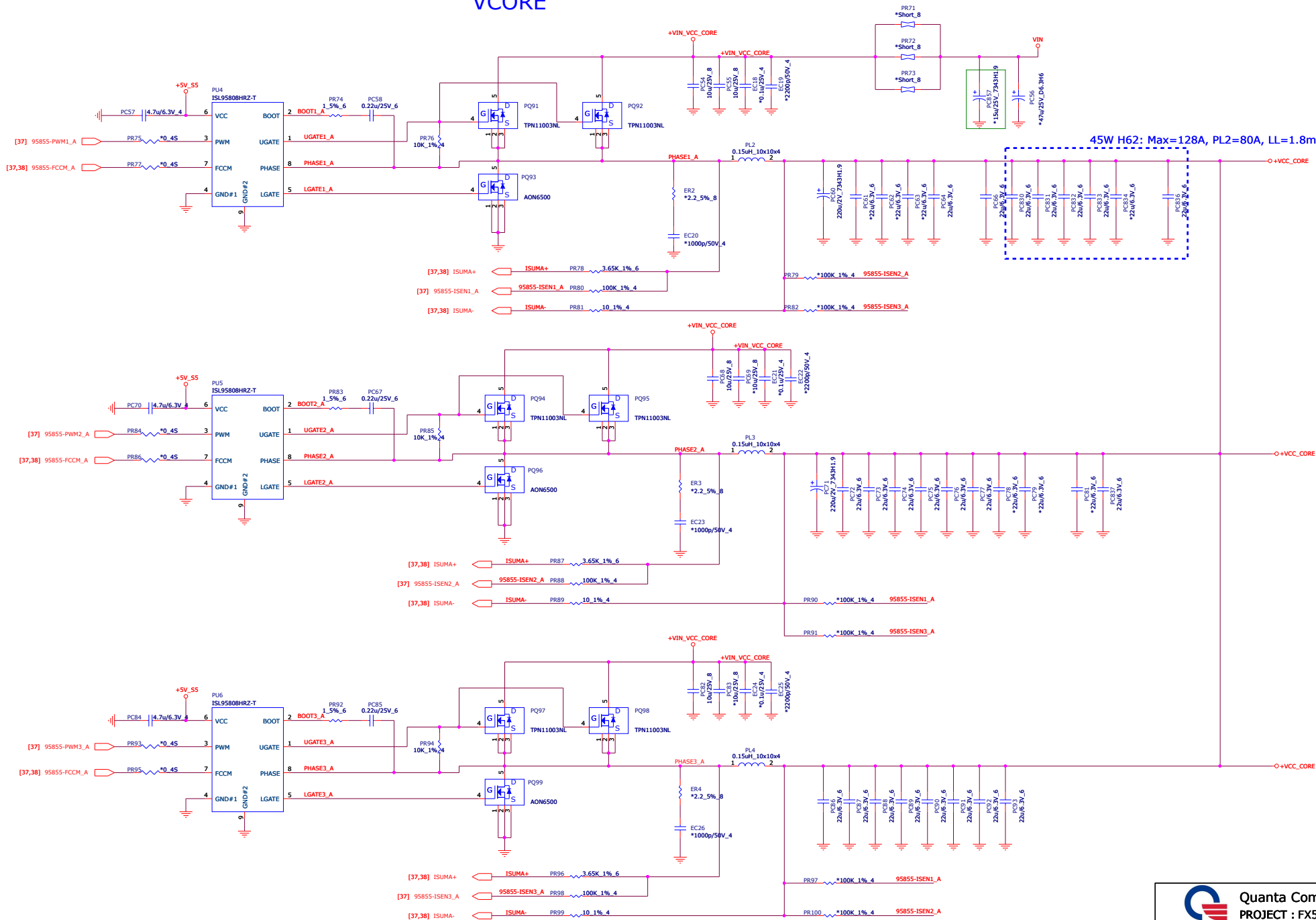
1204 Change

1/18 PR Change

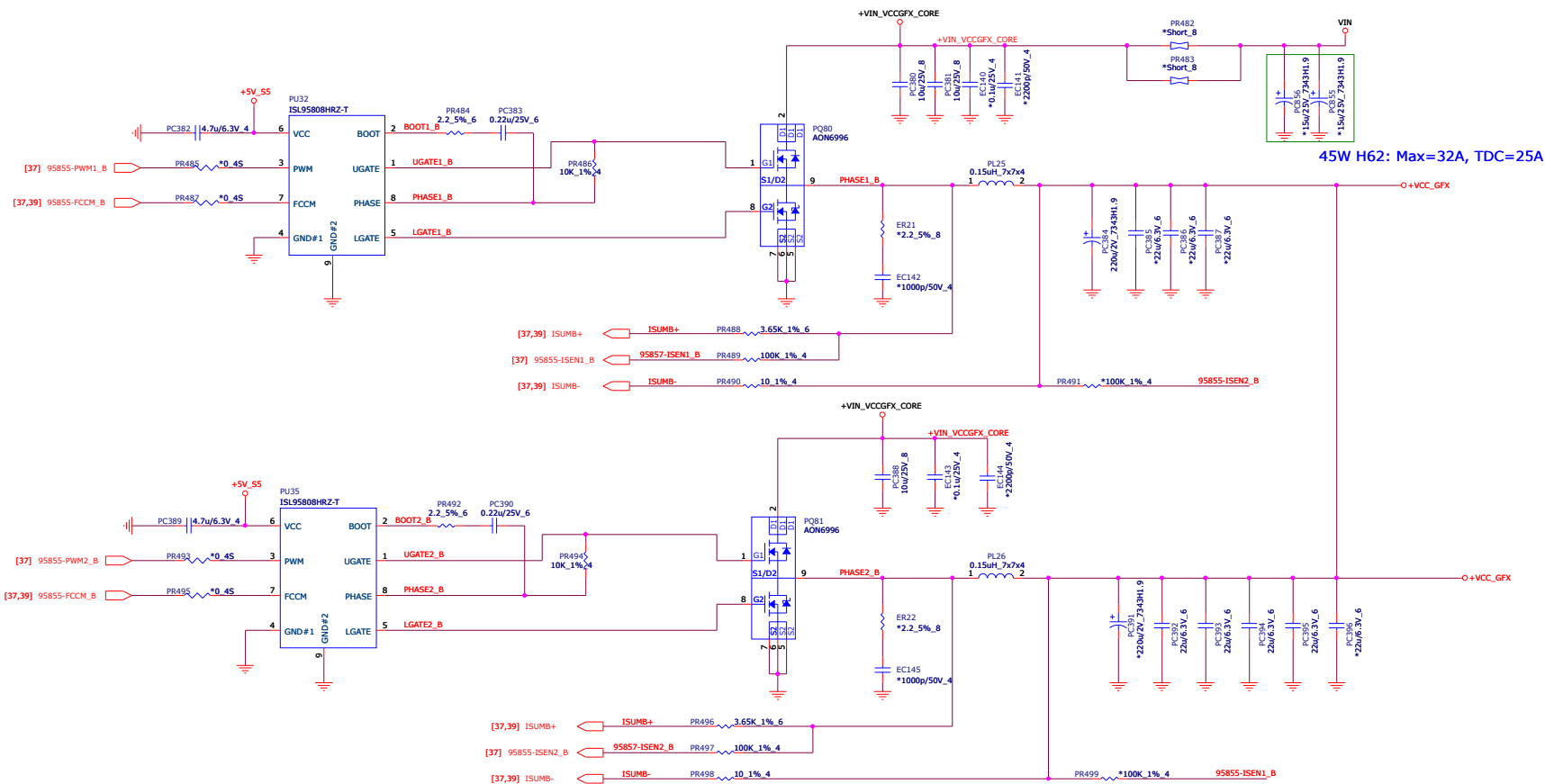


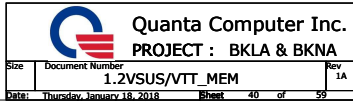


VCORE

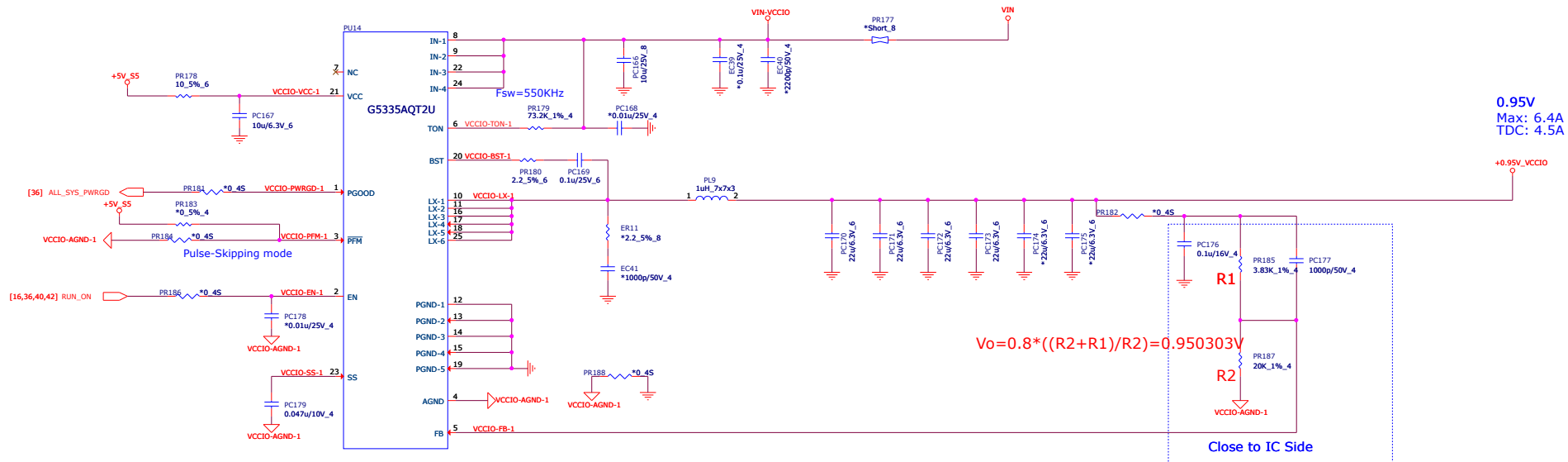


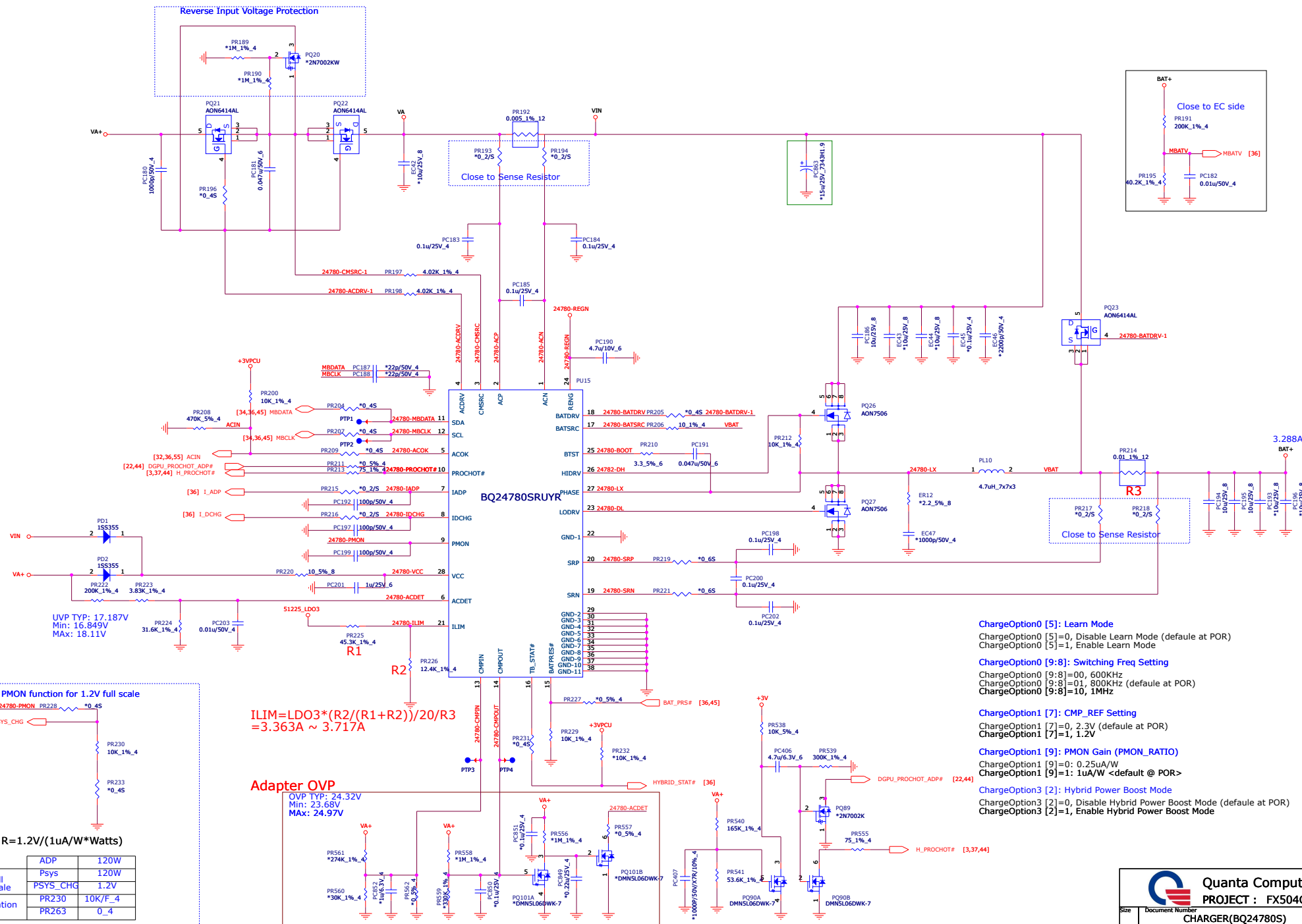
GFX_CORE





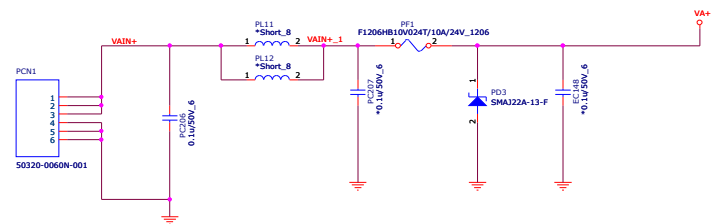
+VCCIO (Fix VCCIO=0.95V)



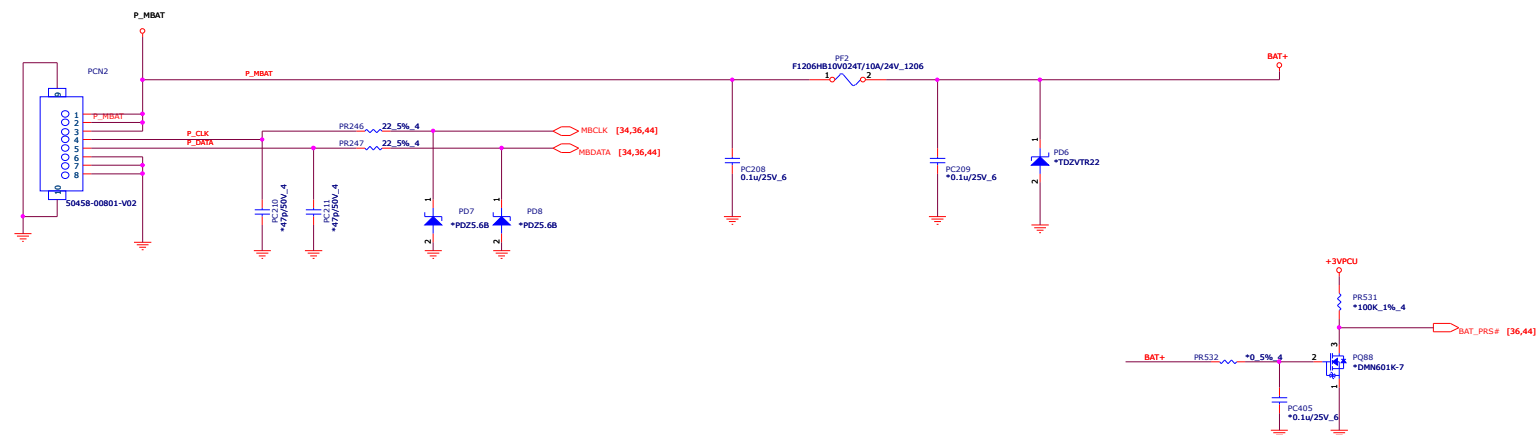


AC IN

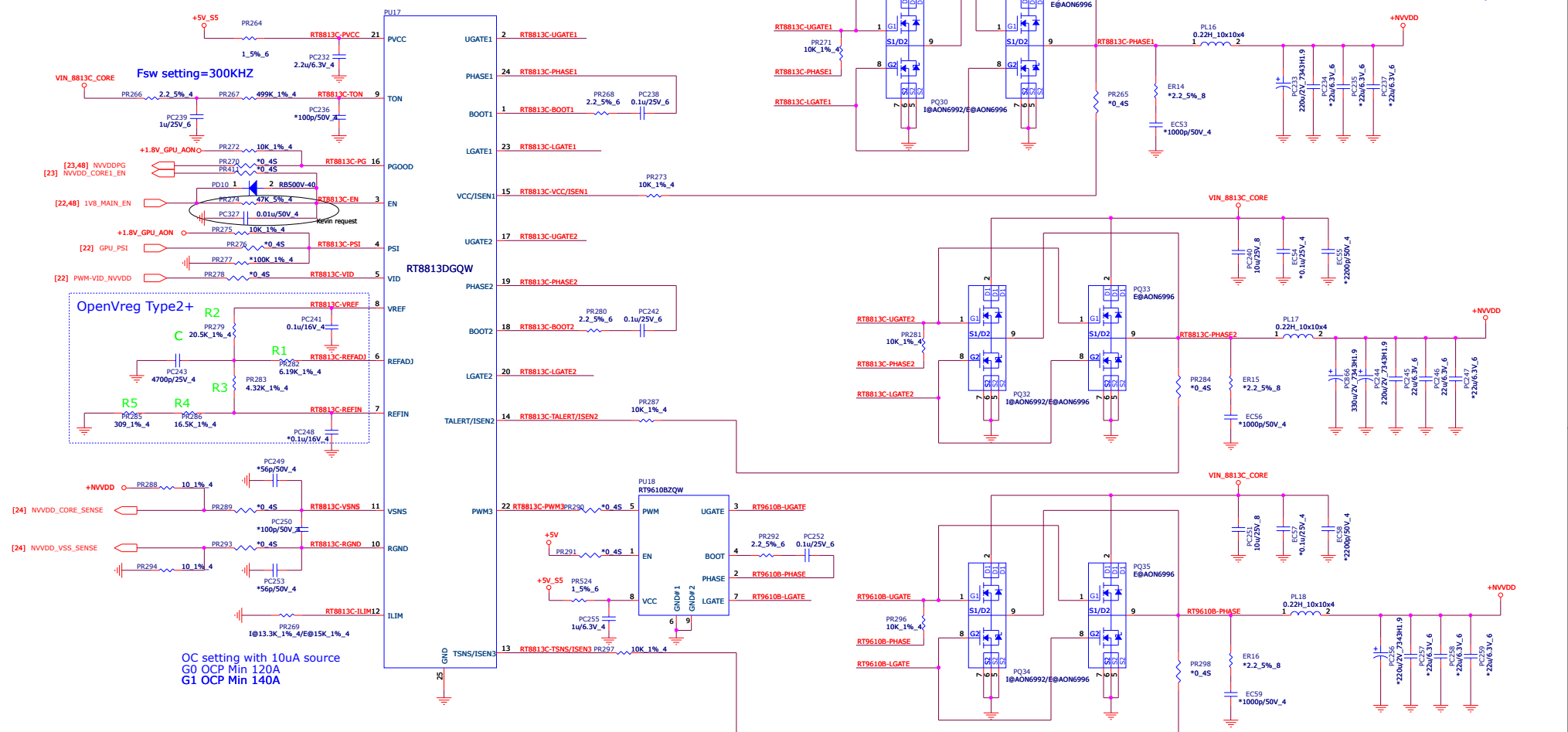
AC ADAPTOR IN CONN



BAT IN

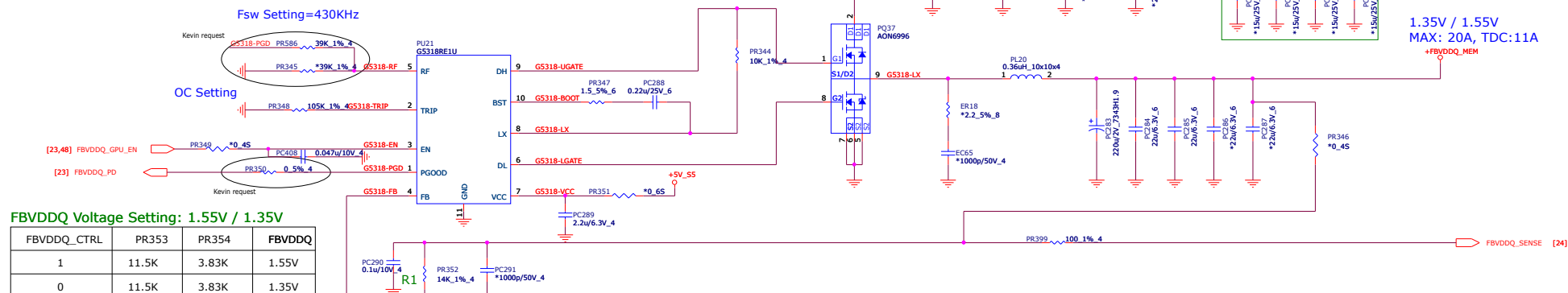


+NVVDD



N17P-G0 (TDP=40W)
 Max=100A, TDC=50A
 N17P-G1 (TDP=50W)
 Max=124A, TDC=59A

FBVDDQ - 1.5V_GPU



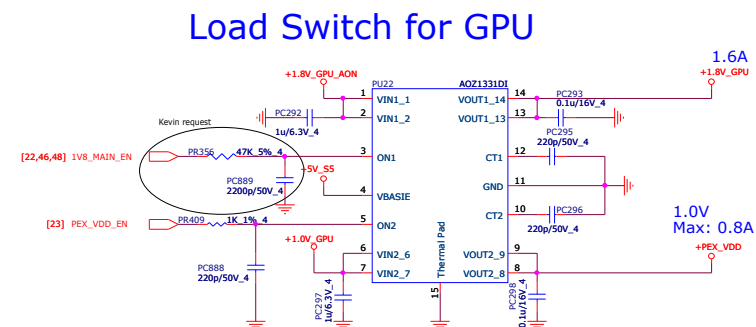
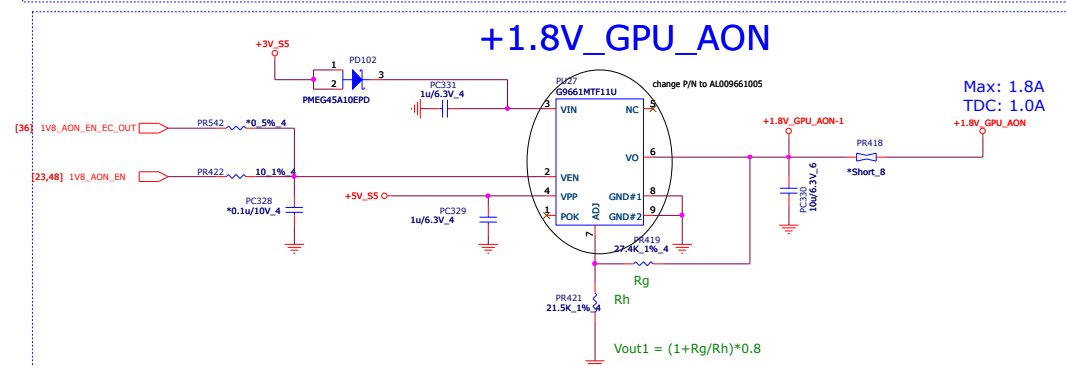
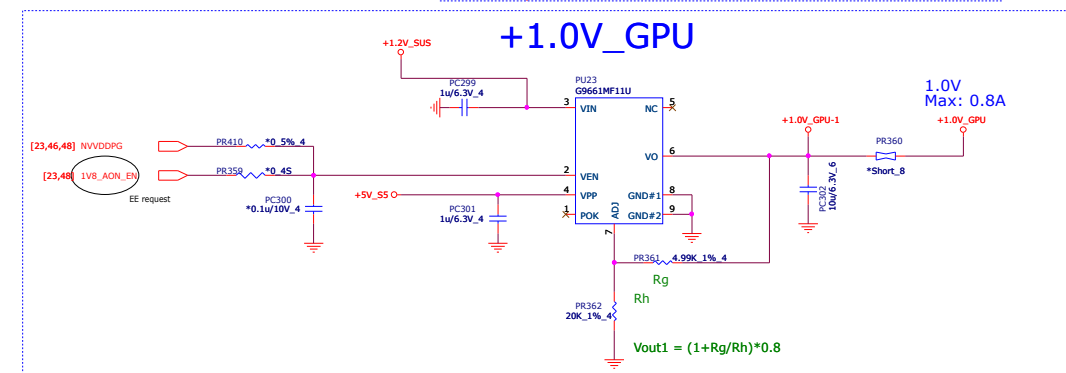
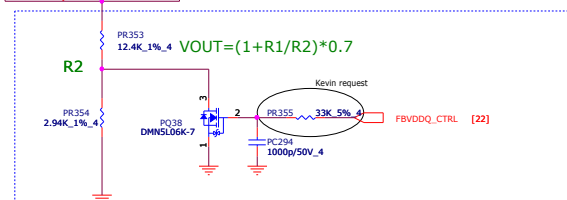
FBVDDQ Voltage Setting: 1.55V / 1.35V

FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	11.5K	3.83K	1.55V
0	11.5K	3.83K	1.35V

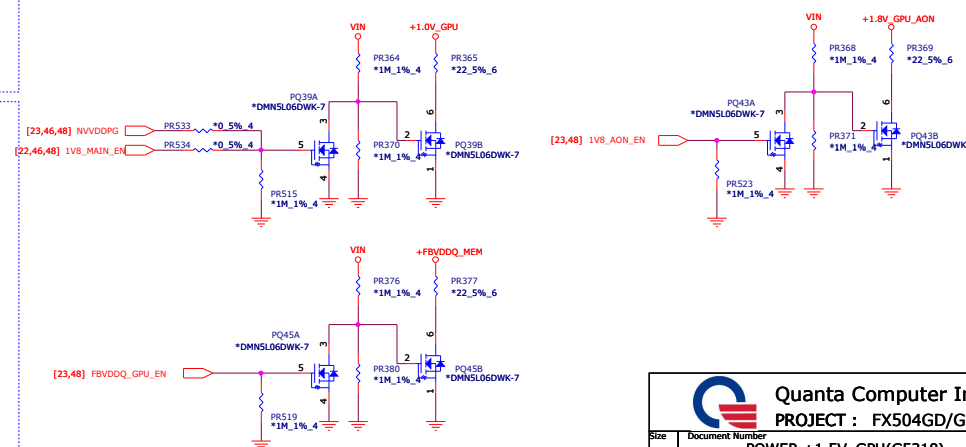
Adjust output to 1.55V/1.35V

FBVDDQ Voltage Setting: 1.50V / 1.35V

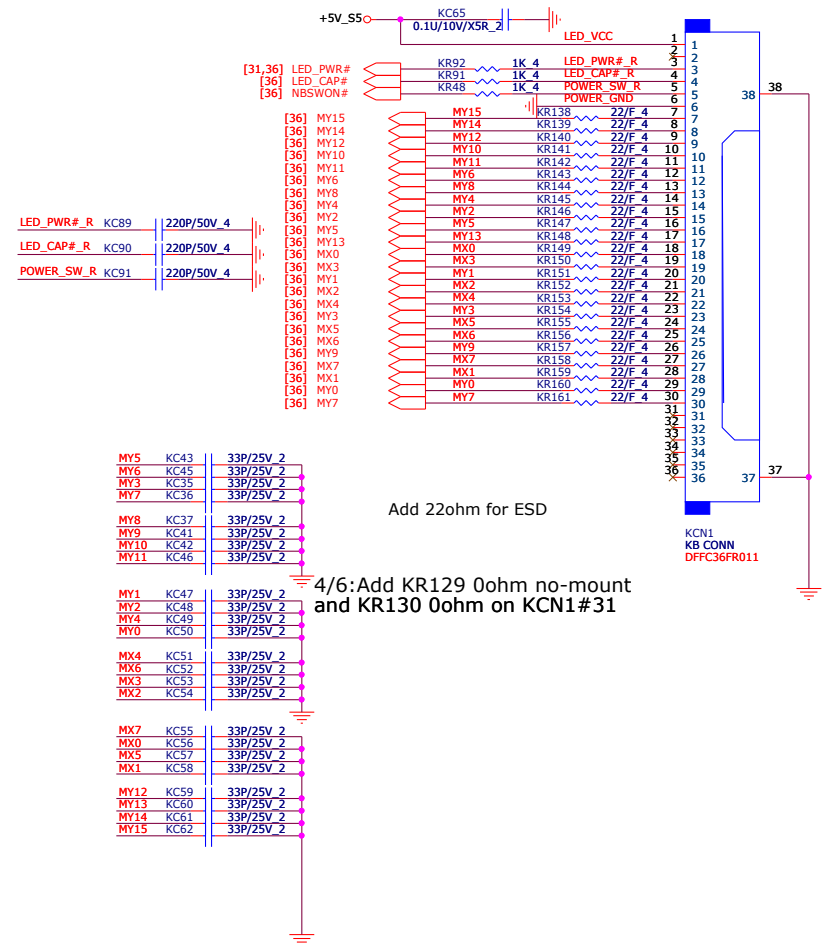
FBVDDQ_CTRL	PR353	PR354	FBVDDQ
1	12.4K	2.94K	1.50V
0	12.4K	2.94K	1.35V



Discharge

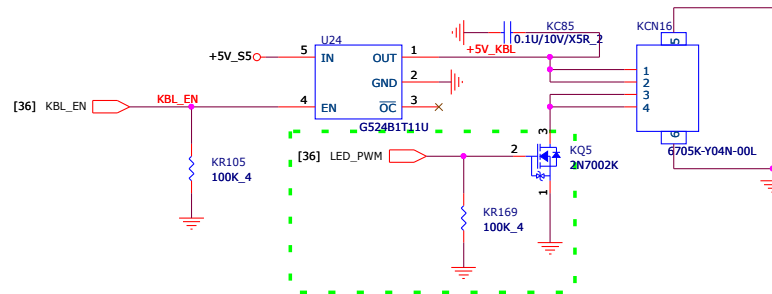


KEYBOARD Con.



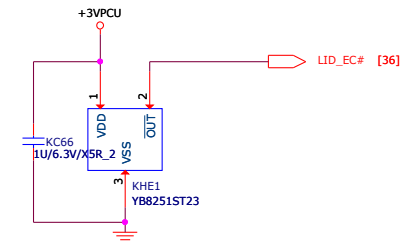
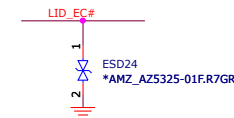
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KEYBOARD BACKLIGHT Con.

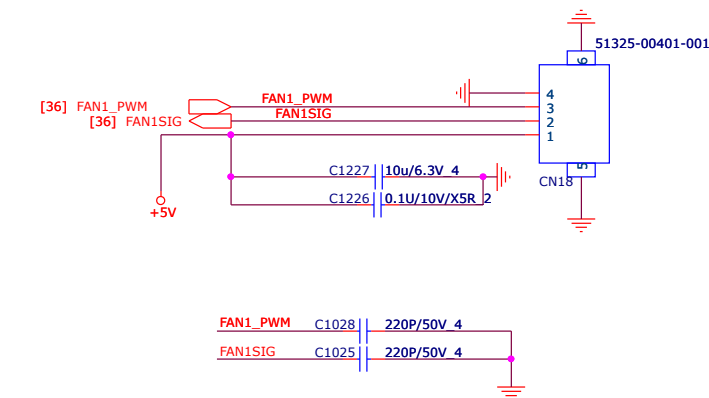


1127 Change

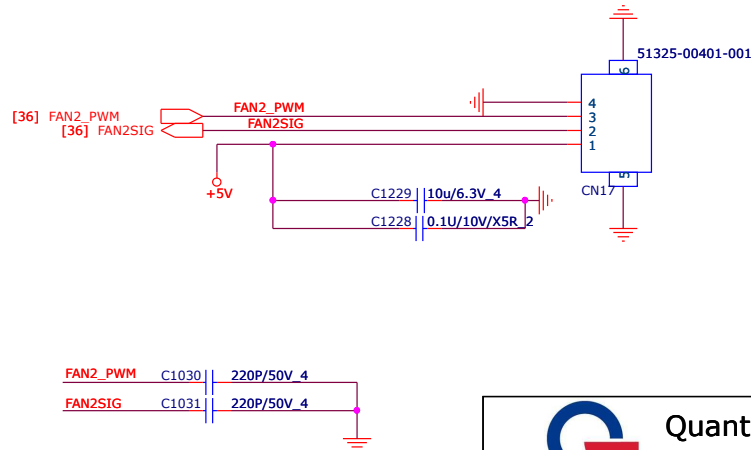
ESD23 CLOSE TO KHE1



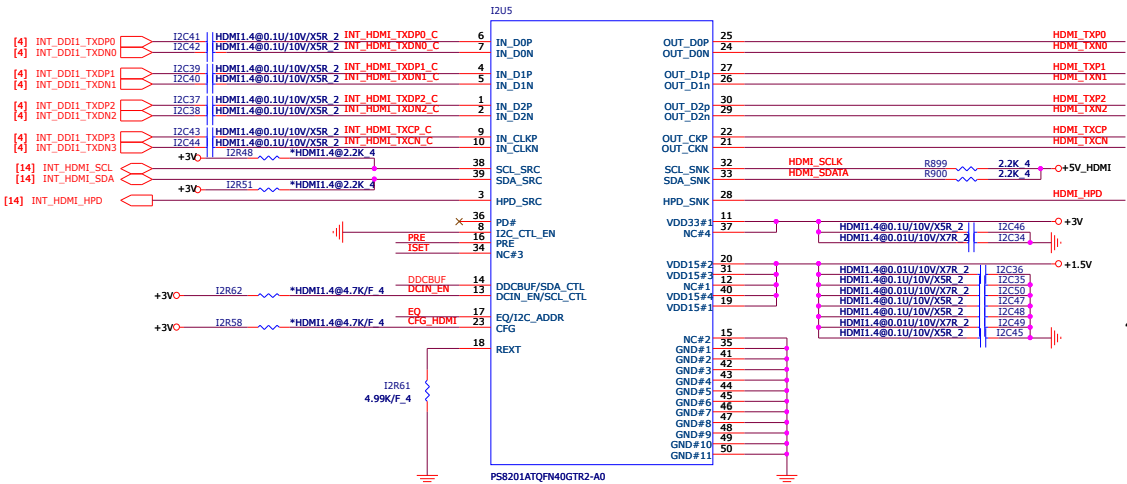
FAN1 for GPU



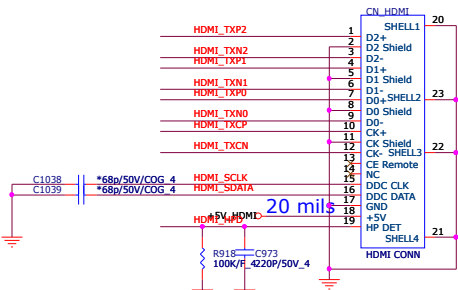
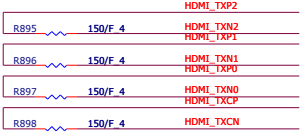
FAN2 for CPU



HDMI 1.4 Re-Drive

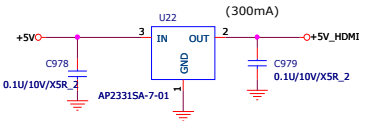


EMI Solution



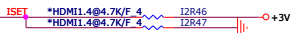
4/5:Change C1038,C1039 from mount 68P to no-mount for EA pass

4/5:Change I2R61 from 3.9K to 4.99K for EA



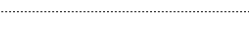
ISET For PS8407A only

TMDS output swing adjustment; Internal pull down at ~150kΩ, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

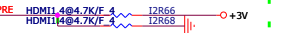


CFG

Configuration pin, 3.3V IO, internal pull down at ~150kΩ, 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable



1124 Change



Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis



EQ For PS8407A

Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 12.4dB
H: programmable EQ for channel loss up to 4.3dB
M: programmable EQ for channel loss up to 8.6dB

EQ For PS8201A

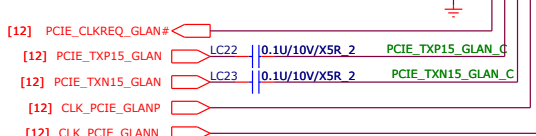
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
L: programmable EQ for channel loss up to 6.5dB @ 3Gbps
H: programmable EQ for channel loss up to 9.5dB @ 3Gbps
M: programmable EQ for channel loss up to 3dB @ 3Gbps

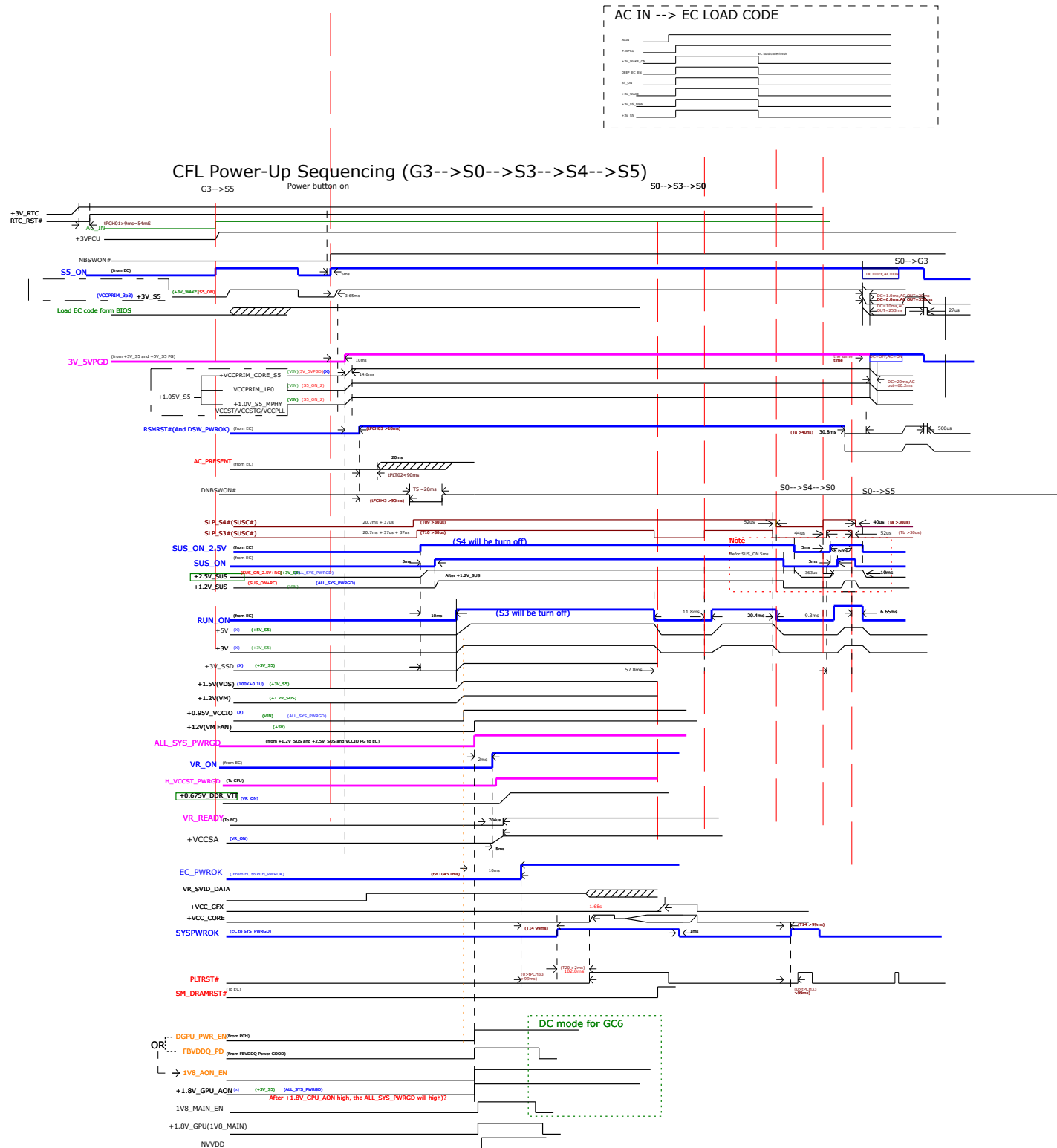
DDCBUF

Enable active DDC buffer; Internal pull down 150Kohm+-20%, 3.3V I/O
L: Passive DDC pass-through (Default)
H: Active DDC buffer with default threshold
M: Active DDC buffer without internal pull up resistor



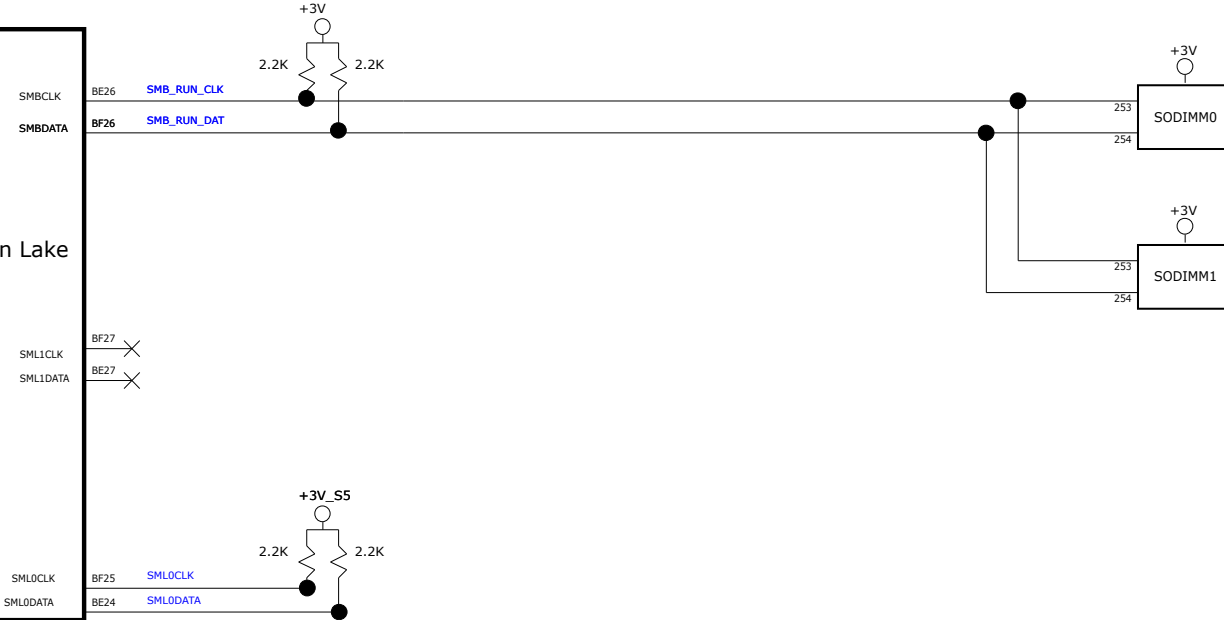






OS status	S0	S3		(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	
H/W status	S0	S3		S4 (Win10 off) RTC wake Enable WOLAN Enable	S4 (Win10 off) RTC wake Disable WOLAN Disable	S5 (Fast Startup "y")	S5 (Fast Startup "x")	
RUN_ON	H	L		L	L	L	L	
+3V	H	L		L	L	L	L	
+5V	H	L		L	L	L	L	
+0.675V_DDR_VTT	H	L		L	L	L	L	
+12V	H	L		L	L	L	L	
+3V_SSD/+3V_PCH_CARD/+1.5V	H	L		L	L	L	L	
+1.05V_VCCSTG	H	L		L	L	L	L	
+VCCSA	H	L		L	L	L	L	
+VCC_GFX	H	L		L	L	L	L	
+VCC_CORE	H	L		L	L	L	L	
+0.95V_VCCIO	H	L		L	L	L	L	
SUS_ON	H	H		L	L	L	L	
+1.05V_VCCPLL/+1.05V_VCCST	H	H		L	L	L	L	
+1.05V_SUS	H	H		L	L	L	L	
+1.2V_SUS	H	H		L	L	L	L	
SUS_ON_2.5V	H	H		L	L	L	L	
+2.5V_SUS	H	H		L	L	L	L	
S5_ON	H	H		H	L	L	L	
+1.8V_S5	H	H		H	L	L	L	
+1.05V_S5	H	H		H	L	L	L	
S5_ON	H	H		H	L	H	L	
+3V_S5	H	H		H	L	H	L	
+5V_S5	H	H		H	L	H	L	

Cannon Lake PCH-H



EC IT8987E

